CMS32F033 User Manual

32-bit microcontrollers based on ARM®Cortex® -M0

Rev. 1.1.3

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1. Product Overview

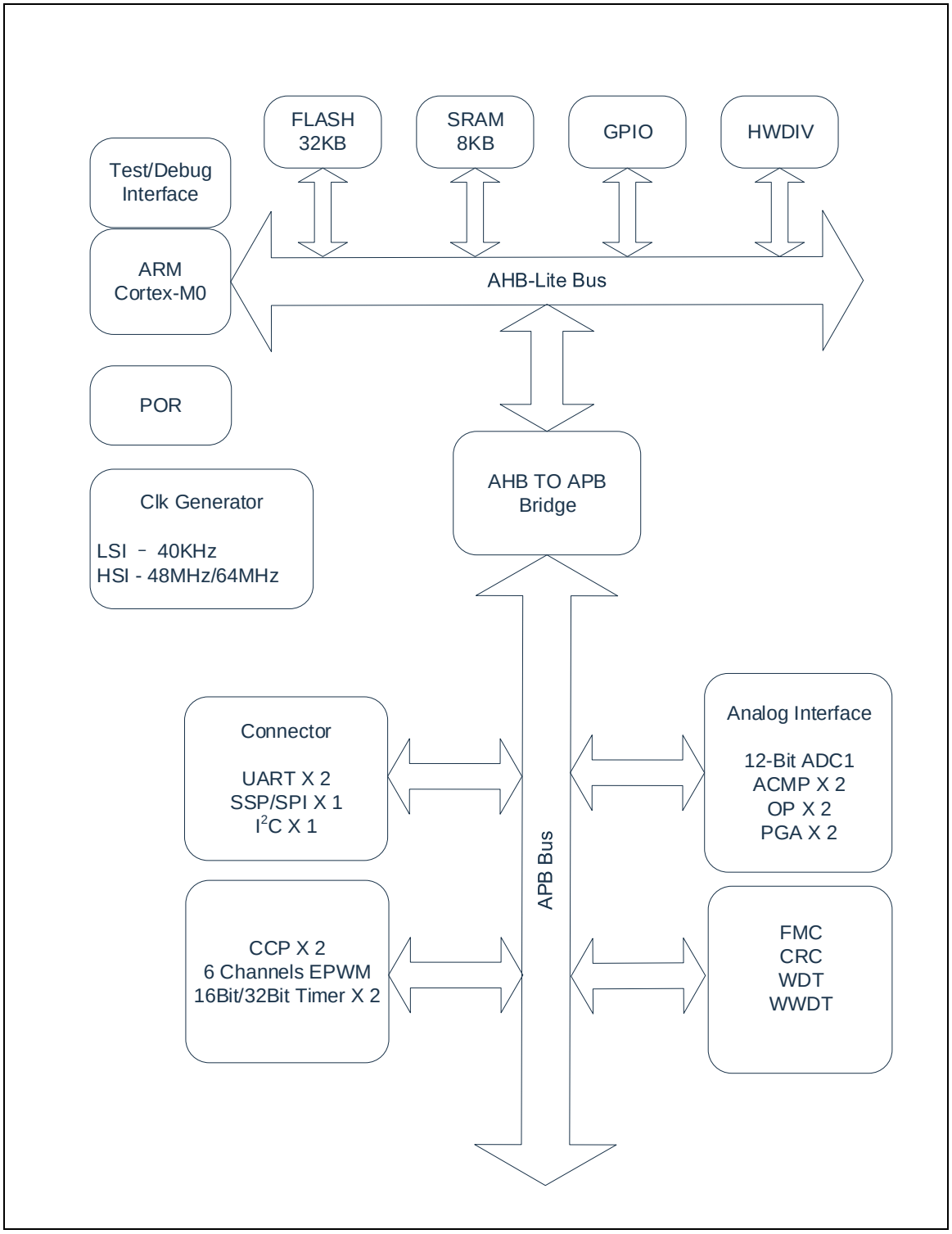
1.1 Features

- **Built in ARM Cortex™-M0, 64MHz@2.1V~5.5V**
  - Single periodic 32-bit hardware multiplier
- **Memory**
  - 32K byte program FLASH (APROM+BOOT)
  - 1K byte FLASH data space (separated space)
  - 8K byte SRAM (support distributed write-protection)
  - Support BOOT function, BOOT unit can be set to 0-4K
  - Support hardware CRC verification FLASH spatial encoding
  - Support FLASH partition protection (min. unit of 2K)
- **System clock**
  - High speed internal clock: 48MHz/64MHz (HSI)
  - Low speed internal clock: 40KHz (LSI)
- **GPIO (max. 30 I/Os)**
- **LVR (1.9V/2.1V/2.6V)**
- **LVD (2.0V/2.2V/2.4V/2.7V/3.0V/3.7V)**
- **System timer**
  - 24-bit SysTick timer
  - Watchdog timer (WDT)
  - Windowed watchdog timer (WWDT)
- **Normal/sleep/deep sleep mode**
- **32-bit hardware divider (HWDIV)**
  - With/without signed mode, divide by zero indication, 6 HCLKs operation completion
- **Cyclic Redundancy Check (CRC)**
- **Timer (32bit/16bit-TIMER0/1)**
- **Capture/Compare/PWM (CCP0/1)**
  - Support 4 channels
- **Communication interface**
  - 1 I^2C module (max. speed of 1Mb/s)
  - 1 SSP/SPI module (4 to 16-bit data format adjustable)
  - 2 UARTs: UART0/1 (total 32 receive/transmit FIFOs)
  - (TXD1 and RXD1 of UART1 can be set to any interfaces)
- **Serial Wire Debug (2-Wire)**
- **96-bit unique ID (UID)**
- **128-bit user UID (USRUID)**
  - User can set and encrypt (can be used as security key)
- **Enhanced PWM (EPWM)**
  - 6 channels
  - Support individual/complementary /synchronized/grouped output mode
  - Support edge/center aligned mode
  - Support single/continuous/interval update mode
  - Support complementary PWM with dead-time insertion (10-bit delay counter)
- **ADC1 (12bit, 1.2Msps)**
  - 30 external channels (all I/Os are supported as AD channels)
  - Each converting channel has separated product registers
  - Support single/continuous/inserting mode
  - Support external trigger mode
  - 1 converted output comparator, can generate interrupt
- **Analog comparator (ACMP0/1)**
  - 4 choices from positive end, negative end can choose internal 1.2V/VDD
  - Support hysteresis voltage selection: 10mV/20mV/60mV
- **Programmable gain amplifier (PGA0/1)**
  - 4 choices in positive end
  - Output can connect to internal ADC channel and the input of analog comparator
  - Internal gain selection: 4x to 32x
- **Operational amplifier (OP0/1)**
  - Input can connect to internal 1.2V
  - Output can connect to internal ADC channel
  - Can set to comparator mode
- **Support security-related applications and functions**

Product description

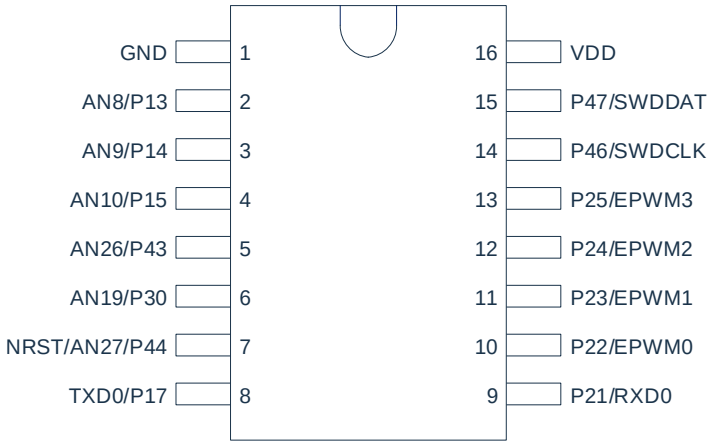
PRODUCT	FLASH	RAM	I/O	12bit-ADC	Timer	CCP	EPWM	SSP	I^2C	UART	OP	PGA	ACMP	PACKAGE
CMS32F033SO16	32K	8K	14	14	2	2	6	1	1	2	1	2	1	SOP16
CMS32F033SS24	32K	8K	22	22	2	2	6	1	1	2	2	2	2	SSOP24
CMS32F033LQ32	32K	8K	27	27	2	2	6	1	1	2	2	2	2	LQFP32
CMS32F033QN32	32K	8K	30	30	2	2	6	1	1	2	2	2	2	QFN32

1.2 System structure



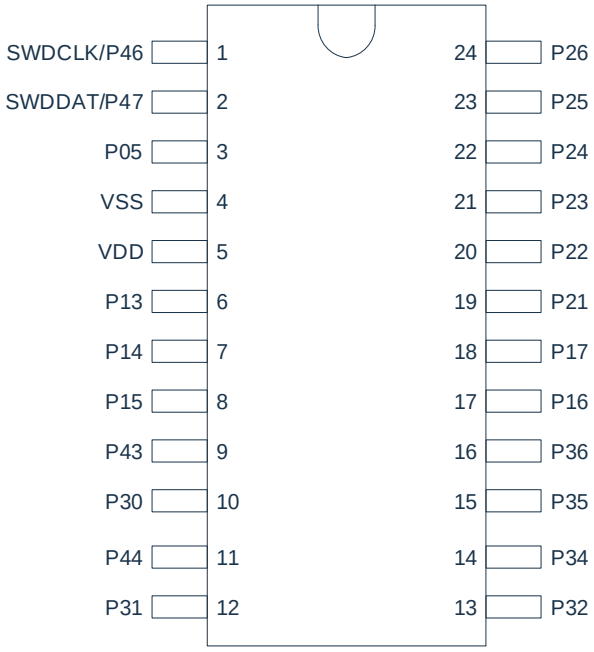
1.3 Pin configuration

1.3.1 CMS32F033SO16



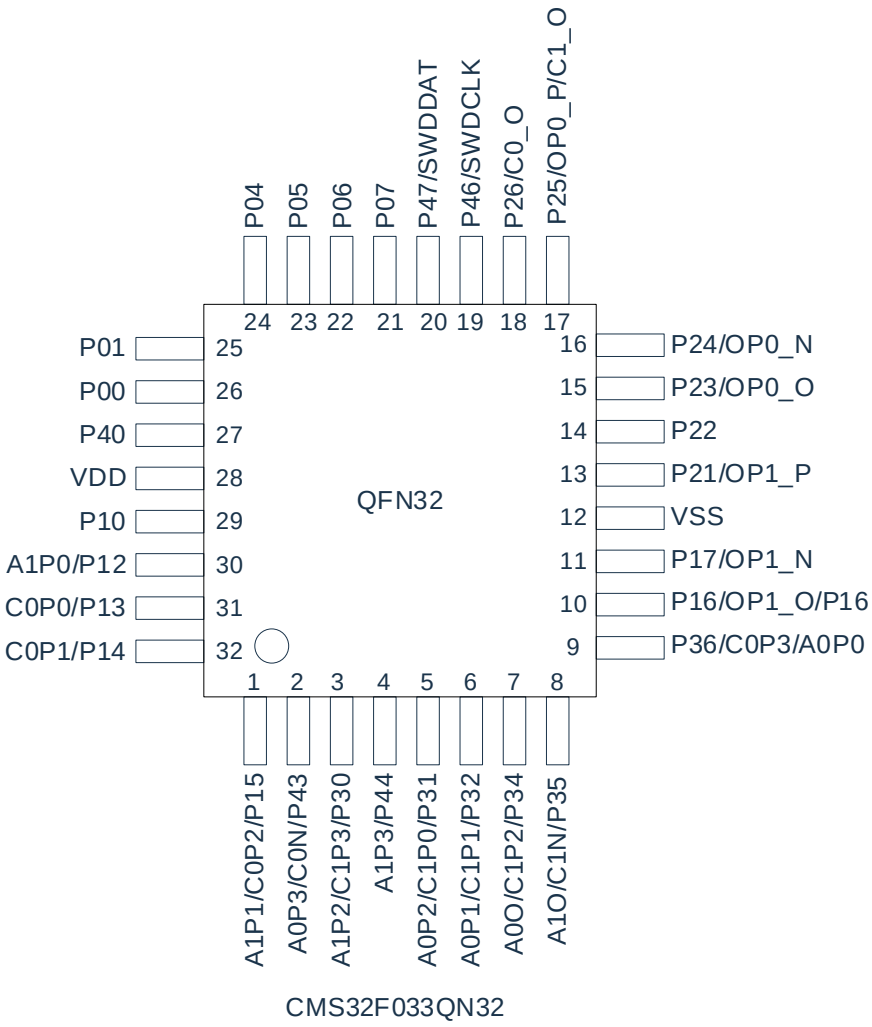
CMS32F033SO16

1.3.2 CMS32F033SS24



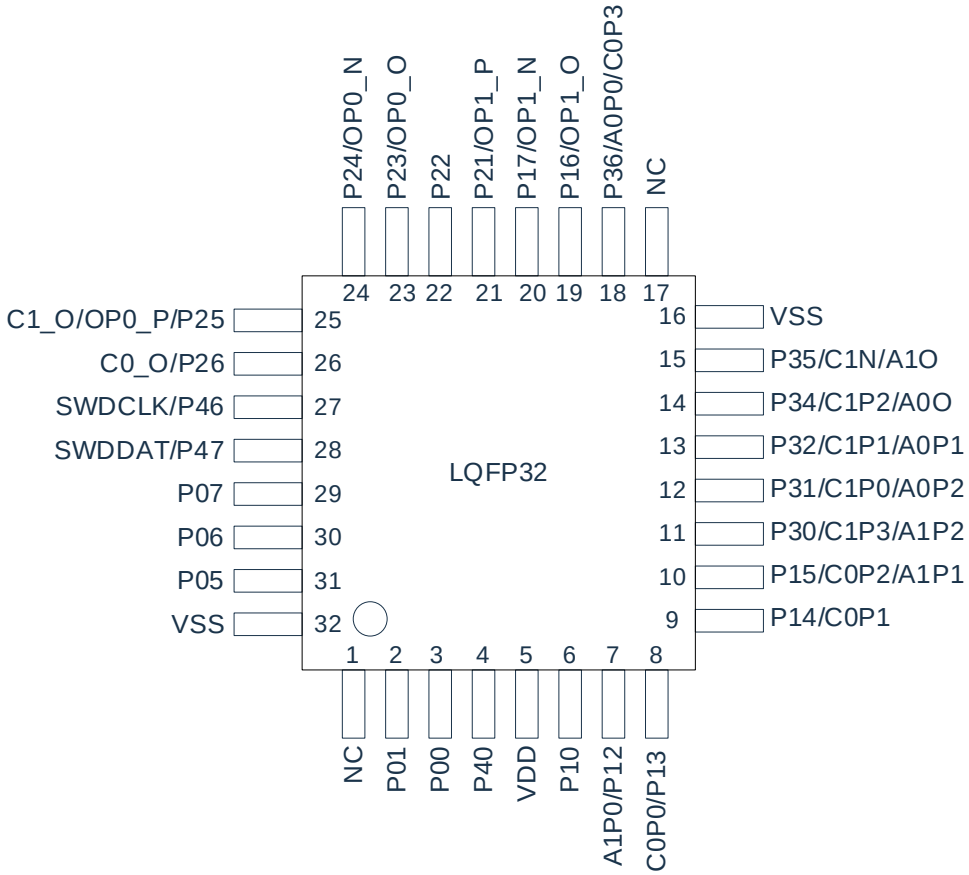
CMS32F033SS24

1.3.3 CMS32F033QN32



CMS32F033QN32

1.3.4 CMS32F033LQ32



CMS32F033LQ32

1.3.5 Analog function pin

Symbol	Description
C0P0	Comparator 0 positive input 0
C0P1	Comparator 0 positive input 1
C0P2	Comparator 0 positive input 2
C0P3	Comparator 0 positive input 3
C0N	Comparator 0 negative input
C1P0	Comparator 1 positive input 0
C1P1	Comparator 1 positive input 1
C1P2	Comparator 1 positive input 2
C1P3	Comparator 1 positive input 3
C1N	Comparator 1 negative input
A0P0	PGA0 positive input 0
A0P1	PGA0 positive input 1
A0P2	PGA0 positive input 2
A0P3	PGA0 positive input 3
A0O	PGA0 output
A1P0	PGA1 positive input 0
A1P1	PGA1 positive input 1
A1P2	PGA1 positive input 2
A1P3	PGA1 positive input 3
A1O	PGA1 output
OP0_P	Operational amplifier 0 positive input
OP0_N	Operational amplifier 0 negative input
OP0_O	Operational amplifier 0 output
OP1_P	Operational amplifier 1 positive input
OP1_N	Operational amplifier 1 negative input
OP1_O	Operational amplifier 1 output
C0_O	Analog comparator 0 digital output
C1_O	Analog comparator 1 digital output

1.3.6 Pin function list

Function symbol									
	CONFIG	0	1	2	3	4	5	6	7
P00		GPIO	--	TXD0	CTS0	SPI0_CLK	CCP0A	EPWM2	-
P01		GPIO	ANA	RXD0	RTS0	SPI0_SS	CCP0B	EPWM0	ADET
P04		GPIO	ANA		CTS1	SPI0_SS	CCP0A	EPWM1	SPI0_CLK
P05	BOOT	GPIO	ANA		RTS1	SPI0_MOSI	CCP0B	EPWM2	ADET
P06		GPIO	ANA		SDA0	SPI0_MISO	CCP1A	EPWM3	CTS1
P07		GPIO	ANA		SCL0	SPI0_CLK	CCP1B	EPWM4	
P10	NRST	GPIO	ANA	TXD0			CCP0A	EPWM1	CTS1
P12		GPIO	ANA	RXD0	SDA0	SPI0_CLK	CCP1B	EPWM0	RTS1
P13		GPIO	ANA	TXD0	SCL0	SPI0_MISO	CCP1A	EPWM1	
P14		GPIO	ANA		SDA0	SPI0_MOSI	CCP0A	EPWM4	
P15		GPIO	ANA		SCL0	SPI0_SS	CCP0A	EPWM5	
P16		GPIO	--	RXD0	SCL0	CTS0	CCP0B	EPWM2	ANA
P17		GPIO	ANA	TXD0	SDA0	RTS0	CCP1A	EPWM4	
P21		GPIO	ANA	RXD0	SCL0		CCP1B	EPWM5	-
P22		GPIO	ANA	TXD0	SCL0	CTS1	CCP0A	EPWM0	SDA0
P23		GPIO	ANA		SDA0	RTS1	CCP0B	EPWM1	-
P24		GPIO	ANA		SDA0		CCP1A	EPWM2	-
P25		GPIO	ANA		SCL0	SPI0_SS	CCP1B	EPWM3	C1_O
P26		GPIO	ANA			SPI0_CLK	CCP0A	EPWM4	C0_O
P30		GPIO	ANA	RXD0	-	SPI0_CLK	CCP0B	EPWM0	ADET
P31		GPIO	ANA	CTS0	SCL0	SPI0_MISO	CCP1A	EPWM4	-
P32		GPIO	ANA	RXD0	SDA0	SPI0_MOSI	CCP1B	EPWM1	-
P34		GPIO	ANA	TXD0	SDA0	SPI0_CLK	CCP0A	EPWM3	-
P35		GPIO	ANA	RTS0	SCL0	SPI0_SS	CCP0B	EPWM5	CLKO
P36		GPIO	ANA			CLKO	CCP1A	EPWM0	-
P40		GPIO	ANA				CCP1B	EPWM1	-
P43	NRST	GPIO	ANA				CCP0A	EPWM2	
P44	NRST	GPIO	ANA	TXD0			CCP0B	EPWM1	
P46		GPIO	ANA	-		SPI0_MISO	CCP1A	EPWM2	SWDCLK0
P47		GPIO	ANA		RTS1	SPI0_MOSI	CCP1B	EPWM5	SWDDAT0

Continued (TXD1 and RXD1 can be configured at any port)

Function symbol					Function symbol			
		8	9	GPIO	ANA (Multiple simulation functions can be used simultaneously)			
PIN	Priority	UART1	UART1	ECAP	ADC1	ACMP	PGA	OP
P00	Max				AN0			
P01	↓				AN1			
P04					AN2			
P05					AN3			
P06					AN4			
P07					AN5			
P10					AN6			
P12					AN7		A1P0	
P13				ECAP00	AN8	C0P0		
P14				ECAP01	AN9	C0P1		
P15				ECAP02	AN10	C0P2	A1P1	
P16					AN11			OP1_O
P17					AN12			OP1_N
P21					AN13			OP1_P
P22					AN14			
P23					AN15			OP0_O
P24		TXD1	RXD1		AN16			OP0_N
P25					AN17			OP0_P
P26	↓				AN18			
P30				ECAP13	AN19	C1P3	A1P2	
P31				ECAP10	AN20	C1P0	A0P2	
P32				ECAP11	AN21	C1P1	A0P1	
P34				ECAP12	AN22	C1P2	A0O	
P35					AN23	C1N	A1O	
P36				ECAP03	AN24	C0P3	A0P0	
P40					AN25			
P43					AN26	C0N	A0P3	
P44	↓				AN27		A1P3	
P46	min				AN28			
P47					AN29			

Note:

1) When the configuration is set to 1, all functions of GPIO, including output circuit and Schmitt input circuit, are closed up and down. When the configuration is 0, that is, when the GPIO function is used, the input Schmitt is normally open (including when the status is output).
2) The port supports the simultaneous use of multiple analog functions. For example, P25 can simultaneously use the op amp function and the AD channel function.
3) When configured as digital function, analog function can also be used. For example, when P13 is

configured as GPIO using ECAP function, comparator C0P0 function can be used at the same time.

4) When using only analog functions, it is recommended to set the configuration to 1 and turn off the digital circuit to reduce power consumption. P00 When using the simulation function, the configuration must be set to GPIO and input mode, and P16 when using the simulation function, the configuration must be set to 7.

Configuration priority of function multi port mapping:

1) Input function

   If two or more ports are configured with the same input function at the same time, configure and select according to the priority order of P00, P01..., P47 from high to low. If P00 and P01 are configured as RXD1 ports at the same time, P00 has high priority. P00 implements RXD1 functions, while P01 is not configured as RXD1 functions.

2) Output function

   The output function has no priority order restriction. If multiple ports are configured with the same output function, the function will output at these ports at the same time.

1.3.7 Pin function description

Pin number			Pin name	Pin type	Description
SSOP24	LQFP32	QFN32			
8	10	1	P15	I/O	General input/output pin
			AN10	AI	ADC analog input channel 10
			C0P2	AI	ACMP0 positive input channel 2
			ECAP02	I	ACMP0 positive input channel 2 as capture input
			A1P1	AI	PGA1 positive input channel 1
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			SCL0	I/O	I2C0 clock input/output pin
			SPI0_SS	I/O	SPI0 slave select pin
			CCP0A	I/O	CCP0 input capture/PWM output A pin
			EPWM5	O	EPWM output channel 5
9	-	2	P43	I/O	General input/output pin
			AN26	AI	ADC analog input channel 26
			C0N	AI	ACMP0 negative input channel
			A0P3	AI	PGA0 positive input channel 3
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			NRST	I	External reset pin
			CCP0A	I/O	CCP0 input capture/PWM output A pin
			EPWM2	O	EPWM output channel 2
10	11	3	P30	I/O	General input/output pin
			AN19	AI	ADC analog input channel 19
			C1P3	AI	ACMP1 positive input channel 3
			ECAP13	I	ACMP1 positive input channel 3 as capture input
			A1P2	AI	PGA1 positive input channel 2
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			RXD0	I	UART0 data input pin
			SPI0_CLK	I/O	SPI0 clock input/output pin
			CCP0B	I/O	CCP0 input capture/PWM output B pin
			EPWM0	O	EPWM output channel 0
			ADET	I	ADC external enable digital input
11	-	4	P44	I/O	General input/output pin
			AN27	AI	ADC analog input channel 27
			A1P3	AI	PGA1 positive input channel 3
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			NRST	I	External reset pin
			TXD0	O	UART0 data output pin
			CCP0B	I/O	CCP0 input capture/PWM output B pin
			EPWM1	O	EPWM output channel 1
12	12	5	P31	I/O	General input/output pin
			AN20	AI	ADC analog input channel 20

Pin number			Pin name	Pin type	Description
SSOP24	LQFP32	QFN32			
			C1P0	AI	ACMP1 positive input channel 0
			ECAP10	I	ACMP1 positive input channel 0 as capture input
			A0P2	AI	PGA0 positive input channel 2
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			CTS0	I	UART0 enable transmit pin
			SCL0	I/O	I2C0 clock input/output pin
			SPI0_MISO	I/O	SPI0 master input/slave output pin
			CCP1A	I/O	CCP1 input capture/PWM output A pin
			EPWM4	O	EPWM output channel 4
13	13	6	P32	I/O	General input/output pin
			AN21	AI	ADC analog input channel 21
			C1P1	AI	ACMP1 positive input channel 1
			ECAP11	I	ACMP1 positive input channel 1 as capture input
			A0P1	AI	PGA0 positive input channel 1
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			RXD0	I	UART0 data input pin
			SDA0	I/O	I2C0 data input/output pin
			SPI0_MOSI	I/O	SPI0 master output/slave input pin
			CCP1B	I/O	CCP1 input capture/PWM output B pin
			EPWM1	O	EPWM output channel 1
14	14	7	P34	I/O	General input/output pin
			AN22	AI	ADC analog input channel 22
			C1P2	AI	ACMP1 positive input channel 2
			ECAP12	I	ACMP1 positive input channel 2 as capture input
			A0O	AO	PGA0output channel
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			TXD0	O	UART0 data output pin
			SDA0	I/O	I2C0 data input/output pin
			SPI0_CLK	I/O	SPI0 clock input/output pin
			CCP0A	I/O	CCP0 input capture/PWM output A pin
			EPWM3	O	EPWM output channel 3
15	15	8	P35	I/O	General input/output pin
			AN23	AI	ADC analog channel 23
			C1N	AI	ACMP1 negative input channel
			A1O	AO	PGA1output channel
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			RTS0	O	UART0 request transmit pin
			SCL0	I/O	SPI0 clock input/output pin
			SPI0_SS	I/O	SPI0 slave select pin
			CCP0B	I/O	CCP0 input capture/PWM output B pin
			EPWM5	O	EPWM output channel 5

Pin number			Pin name	Pin type	Description
SSOP24	LQFP32	QFN32			
			CLKO	O	System clock output pin
16	18	9	P36	I/O	General input/output pin
			AN24	AI	ADC analog channel 24
			C0P3	AI	ACMP0 positive input channel 3
			ECAP03	I	ACMP0 positive input channel 3 as capture input
			A0P0	AI	PGA0 positive input channel 0
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			CCP1A	I/O	CCP1 input capture/PWM output A pin
			EPWM0	O	EPWM output channel 0
			CLKO	O	System clock output pin
17	19	10	P16	I/O	General input/output pin
			AN11	AI	ADC analog channel 11
			OP1_O	AO	OPA1 output channel
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			RXD0	I	UART0 data input pin
			SCL0	I/O	I2C0 clock input/output pin
			CTS0	I	UART0 enable transmit pin
			CCP0B	I/O	CCP0 input capture/PWM output B pin
			EPWM2	O	EPWM output channel 2
18	20	11	P17	I/O	General input/output pin
			AN12	AI	ADC analog channel 12
			OP1_N	AI	OPA1 negative input
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			TXD0	O	UART0 data output pin
			SDA0	I/O	I2C0 data input/output pin
			RTS0	O	UART0 request transmit pin
			CCP1A	I/O	CCP1 input capture/PWM output A pin
			EPWM4	O	EPWM output channel 4
4	16/32	12	VSS	P	Ground
19	21	13	P21	I/O	General input/output pin
			AN13	AI	ADC analog channel 13
			OP1_P	AI	OPA1 positive input
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			RXD0	I	UART0 data input pin
			SCL0	I/O	I2C0 clock input/output pin
			CCP1B	I/O	CCP1 input capture/PWM output B pin
			EPWM5	O	EPWM output channel 5
20	22	14	P22	I/O	General input/output pin
			AN14	AI	ADC analog channel 14
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin

Pin number			Pin name	Pin type	Description
SSOP24	LQFP32	QFN32			
			TXD0	O	UART0 data output pin
			SCL0	I/O	I2C0 clock input/output pin
			CTS1	I	UART1 enable transmit pin
			CCP0A	I/O	CCP0 input capture/PWM output A pin
			EPWM0	O	EPWM output channel 0
			SDA0	I/O	I2C0 data input/output pin
21	23	15	P23	I/O	General input/output pin
			AN15	AI	ADC analog channel 15
			OP0_O	AO	OPA0 output channel
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			SDA0	I/O	I2C0 data input/output pin
			RTS1	O	UART1 request transmit pin
			CCP0B	I/O	CCP0 input capture/PWM output B pin
			EPWM1	O	EPWM output channel 1
22	24	16	P24	I/O	General input/output pin
			AN16	AI	ADC analog channel 16
			OP0_N	AI	OPA0 negative input channel
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			SDA0	I/O	I2C0 data input/output pin
			CCP1A	I/O	CCP1 input capture/PWM output A pin
			EPWM2	O	EPWM output channel 2
23	25	17	P25	I/O	General input/output pin
			AN17	AI	ADC analog channel 17
			OP0_P	AI	OPA0 positive input channel
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			SCL0	I/O	I2C0 clock input/output pin
			SPI0_SS	I/O	SPI0 slave select pin
			CCP1B	I/O	CCP1 input capture/PWM output B pin
			EPWM3	O	EPWM output channel 3
			C1_O	O	ACMP1output channel
24	26	18	P26	I/O	General input/output pin
			AN18	AI	ADC analog channel 18
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			SPI0_CLK	I/O	SPI0 clock input/output pin
			CCP0A	I/O	CCP0 input capture/PWM output A pin
			EPWM4	O	EPWM output channel 4
			C0_O	O	ACMP0output channel
1	27	19	P46	I/O	General input/output pin
			AN28	AI	ADC analog channel 28
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			SPI0_MISO	I/O	SPI0 master input/slave output pin

Pin number			Pin name	Pin type	Description
SSOP24	LQFP32	QFN32			
			CCP1A	I/O	CCP1 input capture/PWM output A pin
			EPWM2	O	EPWM output channel 2
			SWDCLK0	I	SWD programming, debugging clock input pin 0
2	28	20	P47	I/O	General input/output pin
			AN29	AI	ADC analog channel 29
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			RTS1	O	UART1 request transmit pin
			SPI0_MOSI	I/O	SPI0 master output/slave input pin
			CCP1B	I/O	CCP1 input capture/PWM output B pin
			EPWM5	O	EPWM output channel 5
			SWDDAT0	I/O	SWD programming, debugging data input/output pin0
-	29	21	P07	I/O	General input/output pin
			AN5	AI	ADC analog channel 5
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			SCL0	I/O	I2C0 clock input/output pin
			SPI0_CLK	I/O	SPI0 clock input/output pin
			CCP1B	I/O	CCP1 input capture/PWM output B pin
			EPWM4	O	EPWM output channel 4
-	30	22	P06	I/O	General input/output pin
			AN4	AI	ADC analog channel 4
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			SDA0	I/O	I2C0 data input/output pin
			SPI0_MISO	I/O	SPI0 master input/slave output pin
			CCP1A	I/O	CCP1 input capture/PWM output A pin
			EPWM3	O	EPWM output channel 3
			CTS1	I	UART1 enable transmit pin
3	31	23	P05	I/O	General input/output pin
			AN3	AI	ADC analog channel 3
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			RTS1	O	UART1 request transmit pin
			SPI0_MOSI	I/O	SPI0 master output/slave input pin
			CCP0B	I/O	CCP0 input capture/PWM output B pin
			EPWM2	O	EPWM output channel 2
			BOOT	I	BOOT configuration input pin
			ADET	I	ADC external enable digital input
-	-	24	P04	I/O	General input/output pin
			AN2	AI	ADC analog channel 2
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			CTS1	I	UART1 enable transmit pin
			SPI0_SS	I/O	SPI0 slave select pin

Pin number			Pin name	Pin type	Description
SSOP24	LQFP32	QFN32			
			CCP0A	I/O	CCP0 input capture/PWM output A pin
			EPWM1	O	EPWM output channel 1
			SPI0_CLK	I/O	SPI0 clock input/output pin
-	2	25	P01	I/O	General input/output pin
			AN1	AI	ADC analog channel 1
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			RXD0	I	UART0 data input pin
			RTS0	O	UART0 request transmit pin
			SPI0_SS	I/O	SPI0 slave select pin
			CCP0B	I/O	CCP0 input capture/PWM output B pin
			EPWM0	O	EPWM output channel 0
			ADET	I	ADC external enable digital input
--	3	26	P00	I/O	General input/output pin
			AN0	AI	ADC analog channel 0
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			TXD0	O	UART0data output pin
			CTS0	I	UART0 enable transmit pin
			SPI0_CLK	I/O	SPI0 clock input/output pin
			CCP0A	I/O	PWM0 input capture/PWM output A pin
			EPWM2	O	EPWM output channel 2
-	4	27	P40	I/O	General input/output pin
			AN25	AI	ADC analog input channel 25
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			CCP1B	I/O	CCP1 input capture/PWM output B pin
			EPWM1	O	EPWM output channel 1
5	5	28	VDD	P	Power supply
-	6	29	P10	I/O	General input/output pin
			AN6	AI	ADC analog input channel 6
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			TXD0	O	UART0 data output pin
			NRST	I	External reset pin
			CCP0A	I/O	CCP0 input capture/PWM output A pin
			EPWM1	O	EPWM output channel 1
			CTS1	I	UART1 enable transmit pin
-	7	30	P12	I/O	General input/output pin
			AN7	AI	ADC analog input pin 7
			A1P0	AI	PGA1 positive input channel 0
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			RXD0	I	UART0 data input pin
			SDA0	I/O	I2C0 data input/output pin
			SPI0_CLK	I/O	SPI0 clock input/output pin

Pin number			Pin name	Pin type	Description
SSOP24	LQFP32	QFN32			
			CCP1B	I/O	CCP1 input capture/PWM output B pin
			EPWM0	O	EPWM output channel 0
			RTS1	O	UART1 request transmit pin
6	8	31	P13	I/O	General input/output pin
			AN8	AI	ADC analog input pin 8
			C0P0	AI	ACMP0 positive input channel 0
			ECAP00	I	ACMP0 positive input channel 0 as capture input
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			TXD0	O	UART0 data output pin
			SCL0	I/O	I2C0 clock input/output pin
			SPI0_MISO	I/O	SPI0 master input/slave output pin
			CCP1A	I/O	CCP1 input capture/PWM output A pin
			EPWM1	O	EPWM output channel 1
7	9	32	P14	I/O	General input/output pin
			AN9	AI	ADC analog input pin 9
			C0P1	AI	ACMP0 positive input channel 1
			ECAP01	I	ACMP0 positive input channel 1 as capture input
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			SDA0	I/O	I2C0 data input/output pin
			SPI0_MOSI	I/O	SPI0 master output/slave input pin
			CCP0A	I/O	CCP0 input capture/PWM output A pin
			EPWM4	O	EPWM output channel 4

2. System Management

2.1 ARM Cortex–M0 core

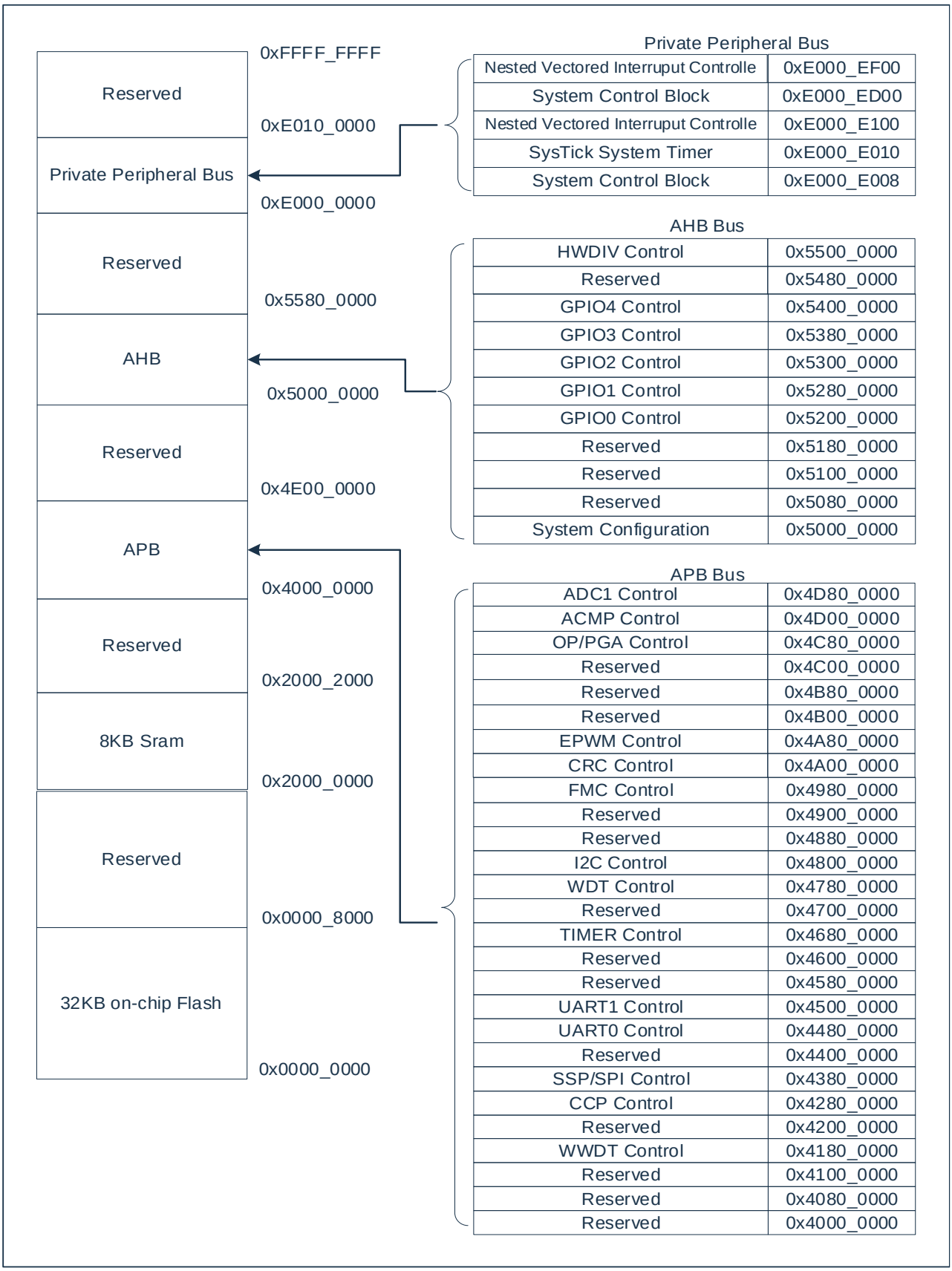
2.1.1 Overview

The Cortex® -M0 is a configurable 32-bit RISC processor with multi-level pipeline. It contains a AMBA AHB-Lite interface which includes NVIC tools and has choice of configurable hardware. This processor can run Thumb instructions and it is compatible with other Cortex® -M processors. It has 2 working modes——Thread mode and Handler mod. When exception happens, system enters Handler mode and exception return is only carried out at Handler mode. After system reset or exception return, the processor can enter Thread mode.

2.1.2 Features

- Low gate count processor:
  - ARMv6-M Thumb® instruction set.
  - Thumb-2 technology.
  - The ARMv6-M is compatible with 24-bit system timers.
  - A 32-bit hardware multiplier.
  - The system interface supports small-endian data access.
  - Accurate and timely interrupt handling capabilities.
  - Loading/storing multiple data and multicycle multiplication instructions can be terminated and then restarted for fast interrupt handling.
  - Exception compatibility mode for the binary interface of the C application.
  - ARMv6-M's C Application Binary Interface (C-ABI) exception compatibility mode allows users to implement interrupt handling using pure C functions.
- NVIC:
  - 32 external interrupts, each with a priority of 4.
  - Dedicated non-maskable interrupts (NMI).
  - Both level and pulse trigger interrupts are supported.
  - Supports interrupt wake-up controllers (WIC) that provide very low-power idle modes.
- Debugging support:
  - Four hardware breakpoints.
  - Two observation points.
  - Program Count Sampling Register (PCSR) for non-intrusive code analysis.
  - Single-step and vector capture capabilities.
- Bus interface:
  - Provide a simple and integrated single 32-bit AMBA-3 AHB-Lite system interface for all system interfaces and memory.
  - Support a single 32-bit slave port for DAP (Debug Access Port).

2.2 Memory mapping



Private Peripheral Bus

Nested Vectored Interruput Controlle	0xE000_EF00
System Control Block	0xE000_ED00
Nested Vectored Interruput Controlle	0xE000_E100
SysTick System Timer	0xE000_E010
System Control Block	0xE000_E008

AHB Bus

HWDIV Control	0x5500_0000
Reserved	0x5480_0000
GPIO4 Control	0x5400_0000
GPIO3 Control	0x5380_0000
GPIO2 Control	0x5300_0000
GPIO1 Control	0x5280_0000
GPIO0 Control	0x5200_0000
Reserved	0x5180_0000
Reserved	0x5100_0000
Reserved	0x5080_0000
System Configuration	0x5000_0000

APB Bus

ADC1 Control	0x4D80_0000
ACMP Control	0x4D00_0000
OP/PGA Control	0x4C80_0000
Reserved	0x4C00_0000
Reserved	0x4B80_0000
Reserved	0x4B00_0000
EPWM Control	0x4A80_0000
CRC Control	0x4A00_0000
FMC Control	0x4980_0000
Reserved	0x4900_0000
Reserved	0x4880_0000
I2C Control	0x4800_0000
WDT Control	0x4780_0000
Reserved	0x4700_0000
TIMER Control	0x4680_0000
Reserved	0x4600_0000
Reserved	0x4580_0000
UART1 Control	0x4500_0000
UART0 Control	0x4480_0000
Reserved	0x4400_0000
SSP/SPI Control	0x4380_0000
CCP Control	0x4280_0000
Reserved	0x4200_0000
WWDT Control	0x4180_0000
Reserved	0x4100_0000
Reserved	0x4080_0000
Reserved	0x4000_0000

2.3 Clock control

2.3.1 Overview

The clock controller provides the clock source for the entire chip, including the system clock and all peripheral clocks. The controller also provides power control through separate clock switches, clock source selection and frequency dividers for power control.

There are 2 different clock sources:

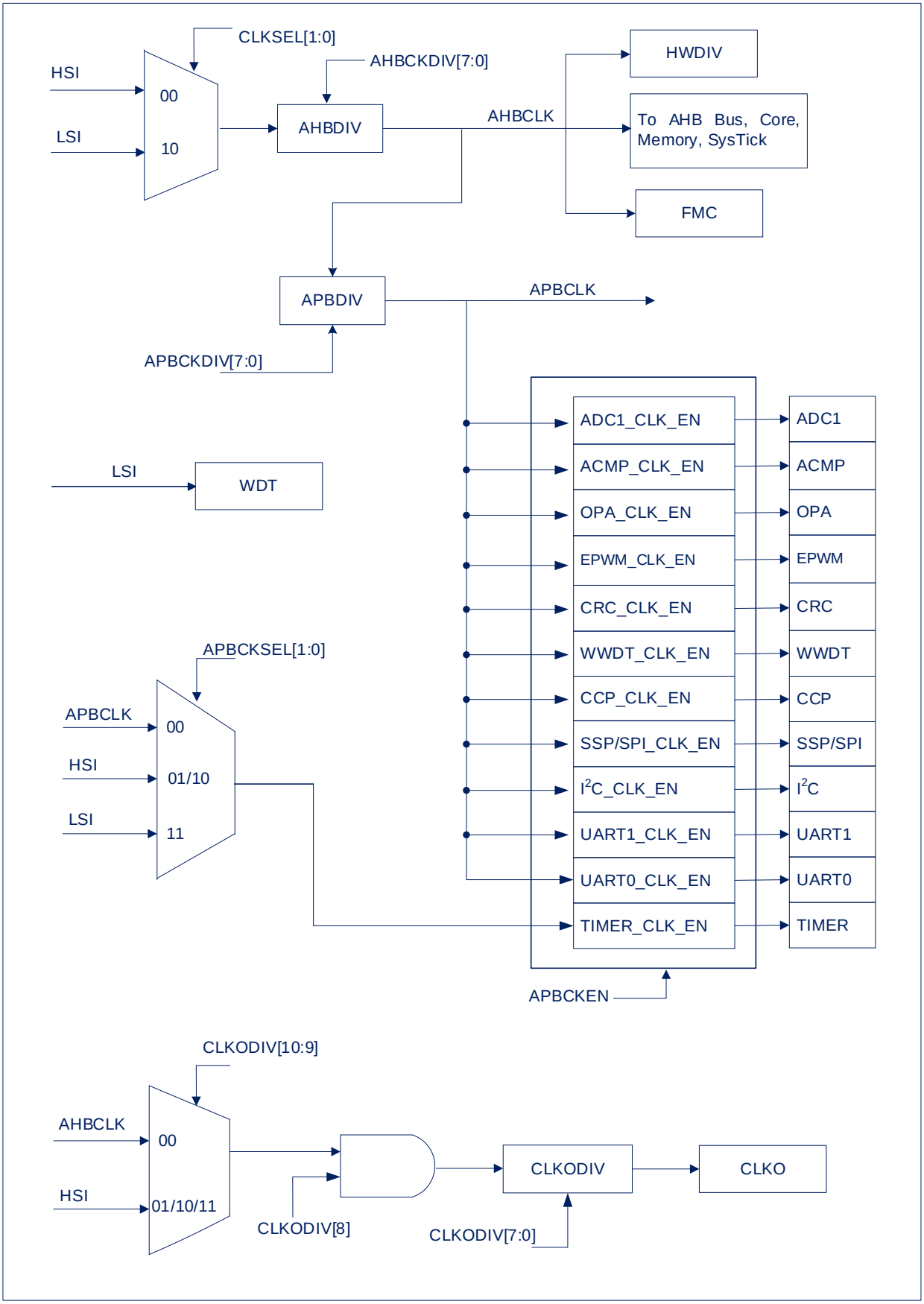
- Internal high-speed clock HSI (48MHz/64MHz).
- Internal low-speed clock LSI (40KHz).

2.3.2 Feature description

2.3.2.1 CLKO function configuration

- Set the P36 or P35 configuration register to the CLKO function.
- Set the CLKODIV register, select the clock source, and divide the output.
- Enable the CLKO output.

2.3.3 Clock control block diagram



2.4 Power management

2.4.1 Overview

The chip has different operating modes to adapt to the power consumption requirements of different applications.

2.4.2 Working mode

The following table lists the available clocks and wake-up sources in different modes.

	Normal mode	Sleep mode (PCON[0]=1)	Deep sleep mode (PCON[1]=1)
Definition	MCU is in normal operation, peripherals are running normally, LDO is on.	MCU is in sleep state, CPU stops working, peripherals run normally, LDO is on	MCU is in deep sleep mode, CPU peripherals except WDT stop working, LDO is on.
Entry condition	Chip in normal mode after system reset is completed	The sleep mode enable bit is set and the CPU executes the WFI command.	The deep sleep mode enable bit is set and the CPU executes the WFI command.
Source of wake-up call	-	All interrupts	I/O interrupt, WDT interrupt
Available clock	-	All clocks except AHBCLK	Internal low-speed 40KHz clock
Post-wakeup mode	-	MCU returns to normal mode, program continues to execute.	MCU returns to normal mode, program continues to execute.
Waiting time after wakeup	-	Run the program now	~25us@Fsys=48MHz
External reset	Support (Reset port hold low >100us reset system)	Support (Reset port hold low >100us reset system)	Support (Reset port held low >100 us reset system)
Low voltage reset	Support	Support	N/A
Low voltage detection	Support	Support	N/A
Low power	-	-	~100uA

2.4.3 Power supply low voltage detection (LVD)

The chip contains an internal low voltage detection circuit, which can detect the voltage of the chip power supply pin VDD.

The detected voltage points can be set to 3.7V/3.0V/2.7V/2.4V/2.2V/2.0V.

2.5 System control (SYSCON)

2.5.1 Overview

System control consists of the following sections:

- System reset.
- System power distribution.
- Sleep mode management.
- System management registers for product ID, chip reset, on-chip controller reset, and multifunction pin control.
- System Timer (SysTick).
- Nested interrupt vector controller (NVIC).
- System control registers.

2.5.2 Register mapping

(SYSCON base address = 0x5000_0000) RO: read only; WO: write only; R/W: read and write.

Register	Offset value	R/W	Description	Reset value
DID	0x000	RO	Product ID register	-
AHBCKDIV	0x004	R/W	AHB clock divider register	0x0
APBCKDIV	0x008	R/W	APB clock divider register	0x0
APBCKEN	0x00C	R/W	APB clock enable register	0xFFFFFFFF
CLKODIV	0x010	R/W	Clock output control registers	0x0
PCON(P0)	0x014	R/W	Power control registers	0x0
RSTCON(P0)	0x018	WO	Reset control registers	0x0
RSTSTAT	0x01C	R/W	Reset status register	-
CLKCON(P0)	0x020	R/W	Clock source control register	0x2F
CLKSEL(P0)	0x024	R/W	Clock source selection register	0x0
CLKSTAT	0x028	RO	Clock source status register	0x1
APBCKSEL	0x02C	R/W	APB clock source selection register	0x0
IOMUX	0x030	RO	IO multiplexed status register	0xFF
CIDL	0x034	RO	UID[63:32]	-
CIDH	0x038	RO	UID[95:64]	-
LVDCON	0x03C	R/W	LVD control register	0x0
IOP00CFG(P1A)	0x040	R/W	P00 configuration register	0x0
IOP01CFG(P1A)	0x044	R/W	P01 configuration register	0x0
-	0x048	-	Reserved	-
-	0x04C	-	Reserved	-
IOP04CFG(P1A)	0x050	R/W	P04 configuration register	0x0
IOP05CFG(P1A)	0x054	R/W	P05 configuration register	0x0
IOP06CFG(P1A)	0x058	R/W	P06 configuration register	0x0
IOP07CFG(P1A)	0x05C	R/W	P07 configuration register	0x0
IOP10CFG(P1A)	0x060	R/W	P10 configuration register	0x0
-	0x064	-	Reserved	-
IOP12CFG(P1A)	0x068	R/W	P12 configuration register	0x0
IOP13CFG(P1A)	0x06C	R/W	P13 configuration register	0x0
IOP14CFG(P1A)	0x070	R/W	P14 configuration register	0x0
IOP15CFG(P1A)	0x074	R/W	P15 configuration register	0x0
IOP16CFG(P1A)	0x078	R/W	P16 configuration register	0x0
IOP17CFG(P1A)	0x07C	R/W	P17 configuration register	0x0
-	0x080	-	Reserved	-
IOP21CFG(P1A)	0x084	R/W	P21 configuration register	0x0
IOP22CFG(P1A)	0x088	R/W	P22 configuration register	0x0
IOP23CFG(P1A)	0x08C	R/W	P23 configuration register	0x0
IOP24CFG(P1A)	0x090	R/W	P24 configuration register	0x0
IOP25CFG(P1A)	0x094	R/W	P25 configuration register	0x0
IOP26CFG(P1A)	0x098	R/W	P26 configuration register	0x0
-	0x09C	-	Reserved	-
IOP30CFG(P1A)	0x0A0	R/W	P30 configuration register	0x0
IOP31CFG(P1A)	0x0A4	R/W	P31 configuration register	0x0
IOP32CFG(P1A)	0x0A8	R/W	P32 configuration register	0x0
-	0x0AC	-	Reserved	-

Register	Offset value	R/W	Description	Reset value
IOP34CFG(P1A)	0x0B0	R/W	P34 configuration register	0x0
IOP35CFG(P1A)	0x0B4	R/W	P35 configuration register	0x0
IOP36CFG(P1A)	0x0B8	R/W	P36 configuration register	0x0
-	0x0BC	-	Reserved	-
IOP40CFG(P1A)	0x0C0	R/W	P40 configuration register	0x0
-	0x0C4	-	Reserved	-
-	0x0C8	-	Reserved	-
IOP43CFG(P1A)	0x0CC	R/W	P43 configuration register	0x0
IOP44CFG(P1A)	0x0D0	R/W	P44 configuration register	0x0
-	0x0D4	-	Reserved	-
IOP46CFG(P1A)	0x0D8	R/W	P46 configuration register	0x0
IOP47CFG(P1A)	0x0DC	R/W	P47 configuration register	0x0
-	-	-	-	-
SYS_IMSC	0x100	R/W	System detect interrupt enable register	0x0
SYS_RIS	0x104	RO	System detect interrupt source status register	0x0
SYS_MIS	0x108	RO	System detect enabled interrupt status register	0x0
SYS_ICLR	0x10C	WO	System detect interrupt clear register	0x0
HSI_TRIM(P0)	0x110	R/W	Internal oscillation frequency trimming register	-
-	-	-	-	-
SRAMLOCK(P0)	0x1B0	R/W	SRAM write protect register	0x0
GPIO0LOCK	0x1C0	R/W	GPIO0 write enable register	0x0
GPIO1LOCK	0x1C4	R/W	GPIO1 write enable register	0x0
GPIO2LOCK	0x1C8	R/W	GPIO2 write enable register	0x0
GPIO3LOCK	0x1CC	R/W	GPIO3 write enable register	0x0
GPIO4LOCK	0x1D0	R/W	GPIO4 write enable register	0x0
IOCFGLOCK	0x1FC	R/W	Port configuration write enable register	0x0
-	-	-	-	-
UIDX	0x500	RO	UID[31:0]	-
PCRCD	0x510	RO	Program check code	
UUIDWC0	0x520	CHK	Detect USRID[31:0]	0x0
UUIDWC1	0x524	CHK	Detect USRID[63:32]	0x0
UUIDWC2	0x528	CHK	Detect USRID[95:64]	0x0
UUIDWCS	0x52C	CHK	Detect fixed code	0x0

Note:

1) (P0/P1D) The registers labeled are protected registers.
2) (P0): When the marked register writes a valid control bit, other bits need to be written to a fixed value, otherwise the write operation is invalid, see the register description.
3) (P1A): When IOCFGLock=99H, the marked register is allowed to write; = Other values, forbidden to write.

2.5.3 Register description

2.5.3.1 Product ID register (DID)

Bit	Symbol	Description	Reset value
31:16	DNO	Core ID	0x4B02
15:0	-	Reserved	-

2.5.3.2 AHB clock divider register (AHBCKDIV)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	AHBDIV	AHB clock division bit 0: HCLK = F_{SYS} 1~255: HCLK = F_{SYS}/(2×AHBDIV)	0x0

2.5.3.3 APB clock divider register (APBCKDIV)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	APBDIV	APB clock division bit 0: PCLK = HCLK 1~255: PCLK = HCLK/(2×APBDIV)	0x0

2.5.3.4 APB clock enable register (APBCKEN)

Bit	Symbol	Description	Reset value
31:28	-	Reserved	-
27	ADC1CE	ADC1 clock enable bit 0: Disable 1: Enable	1
26	ACMPCE	ACMP clock enable bit 0: Disable 1: Enable	1
25	OP/PGACE	OP/PGA clock enable bit 0: Disable 1: Enable	1
24:22	-	Reserved	-
21	EPWMCE	EPWM clock enable bit 0: Disable 1: Enable	1
20	CRCCE	CRC clock enable bit 0: Disable 1: Enable	1
19:15	-	Reserved	-
14	WWDTCE	WWDT clock enable bit 0: Disable 1: Enable	1
13	-	Reserved	-
12	CCPCE	Capture/PWM clock enable bit 0: Disable 1: Enable	1
11:10	-	Reserved	-
9	SSP/SPICE	SSP/SPI clock enable bit 0: Disable 1: Enable	1
8	-	Reserved	-
7	I2CCE	I2C clock enable bit 0: Disable 1: Enable	1
6:5	-	Reserved	-
4	UART1CE	UART1 clock enable bit 0: Disable 1: Enable	1
3	UART0CE	UART0 clock enable bit 0: Disable 1: Enable	1
2	HWDIVCE	HWDIV clock enable bit 0: Disable 1: Enable	1
1	TIMER01CE	TIMER01 clock enable bit 0: Disable 1: Enable	1
0	WDTCE	WDT clock enable bit 0: Disable 1: Enable	1

2.5.3.5 Clock output control register (CLKODIV)

Bit	Symbol	Description	Reset value
31:11	-	Reserved	-
10:9	CLK_SEL	F_{SEL} clock source select bit 00: AHBCLK 01: HSI 02: HSI 03: HSI	0
8	EN	Clock output enable bit 0: Disable CLKO function 1: Enable CLKO function	0
7:0	DIV	Clock output divider 0: $F_{CLKO}=F_{SEL}$ 1~255: $F_{CLKO}=F_{SEL}/(2\times DIV)$	0x0

2.5.3.6 Power control register (PCON)

Bit	Symbol	Description	Reset value
31:16	Key	0x5A69 needs to be written at the same time to operate on the other bits of the register	0x0
15:2	-	Set to 0	-
1	Deep sleep mode	Deep sleep mode enable 0: Disable deep sleep mode 1: Enable Deep sleep mode, and executing WFI instructions will enter deep sleep mode	0x0
0	Sleep mode	Sleep mode enable bit 0: Disable sleep mode 1: Enable sleep mode, and executing WFI instructions will enter sleep mode	0x0

2.5.3.7 Reset control register (RSTCON)

Bit	Symbol	Description	Reset value
31:2	RSTKEY	0x156A99A6 needs to be written at the same time to operate on the other bits of this register, and the read value is 0	0x0
1	CPURST	Write 1 to reset the Cortex-M0 CPU and FMC module (do not load the boot configuration). Writing 0 does not affect	0x0
0	MCURST	Write 1 reset MCU (reload boot configuration) Writing 0 does not affect	0x0

Note: Writing 0x55AA6699 produces MCURST; writing 0x55AA669A produces CPURST.

2.5.3.8 Reset status register (RSTSTAT)

Bit	Symbol	Description	Reset value
31:3	-	Reserved	-
2	CPURS	CPU reset state 0: No CPU reset detected 1: CPU reset detected	-
1	MCURS	MCU reset state 0: No MCU reset detected 1: MCUU reset detected	-
0	WDTRS	WDT reset state 0: No WDT reset detected 1: WDT reset detected	-

2.5.3.9 Clock source control register (CLKCON)

Bit	Symbol	Description	Reset value
31:16	Key	0x5A69 needs to be written at the same time to operate on the other bits of the register	0x0
15:4	-	Reserved	-
3	IRCEN	Internal high-speed oscillation (HSI) enable bit 0: Disable Internal high-speed oscillation 1: Enable internal high-speed oscillation Note: The AHB clock source is selected as HSI or when operating Flash, the system automatically enables HSI, regardless of this bit.	1
2	-	Reserved	1
1:0	IRCSEL	Internal high-speed oscillation (HSI) frequency select bit 00: 64MHz 01: -- 10: -- 11: 48MHz Note: When switching different HSI frequencies, it takes about 125us (4 to 5) × T_{LSI} to switch to the selected frequency, during which the CPU is suspended.	0x3

2.5.3.10 Clock source selection register (CLKSEL)

Bit	Symbol	Description	Reset value
31:16	KEY	The 0x5A69 needs to be written at the same time to operate on the other bits of the register	0x0
15:2	-	Reserved	-
1:0	CLKSEL	AHB clock source select bit 0x0: Internal high-speed oscillation (HSI) 0x1: Write disabled 0x2: Internal 40KHz low-speed oscillation (LSI) 0x3: Write disabled Note: Write disable means that the data cannot be written, CLKSEL still selects the previous oscillator.	0x0

2.5.3.11 Clock source status register (CLKSTAT)

Bit	Symbol	Description	Reset value
31:1	-	Reserved	-
0	IRCSTB	Internal high-speed oscillation (HSI) status bit 0: Internal high-speed oscillation is prohibited or unstable 1: Internal high-speed oscillation is stable (HSI is selected by default at power-up) Note: (HSI requires a settling time of about 4 to 6us from off to on). The conditions included are: - The AHB clock is switched from LSI to HSI - The low-power mode switches to HSI operating mode - The system waits for the HSI to stabilize before supplying its clock to the core	0x1

2.5.3.12 APB clock selection register (APBCKSEL)

Bit	Symbol	Description	Reset value
31:2	-	Reserved	-
1:0	TMR01SEL	Timer 0/1 clock source select bit 0x0: APBCLK 0x1: Internal high-speed oscillation (HSI) 0x2: HSI 0x3: Internal 40KHz low speed oscillation (LSI)	0x0

2.5.3.13 IO multiplexed status register (IOMUX)

Bit	Symbol	Description	Reset value
31:12	-	Reserved	-
11:10	RESETPORT	The external reset pin function is read-only 11: External reset disabled 10: P10 acts as an external reset port 01: P44 acts as an external reset port 00: P43 acts as an external reset port	-
9:0	-	Reserved	-

2.5.3.14 LVD control register (LVDCON)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	-	LVD sense voltage selection bit 000: 2.0V 001: 2.2V 010: 2.4V 011: 2.7V 100: 3.0V 101: 3.7V 110: Reserved 111: Reserved Other: Reserved	0x0

2.5.3.15 P00 configuration tegister (IOP00CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP00CFG	P00 feature selection 0x0: GPIO/AN0 (The AN0 function needs to be set to input) 0x1: - 0x2: TXD0 0x3: CTS0 0x4: SPI0_CLK 0x5: CCP0A 0x6: EPWM2 0x7: - 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.16 P01 configuration register (IOP01CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP01CFG	P01 feature selection 0x0: GPIO 0x1: AN1 0x2: RXD0 0x3: RTS0 0x4: SPI0_SS 0x5: CCP0B 0x6: EPWM0 0x7: ADET 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.17 P04 configuration register (IOP04CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP04CFG	P04 feature selection 0x0: GPIO 0x1: AN2 0x2: - 0x3: CTS1 0x4: SPI0_SS 0x5: CCP0A 0x6: EPWM1 0x7: SPI0_CLK 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.18 P05 configuration register (IOP05CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP05CFG	P05 feature selection 0x0: GPIO 0x1: AN3 0x2: - 0x3: RTS1 0x4: SPI0_MOSI 0x5: CCP0B 0x6: EPWM2 0x7: ADET 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.19 P06 configuration register (IOP06CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP06CFG	P06 feature selection 0x0: GPIO 0x1: AN4 0x2: - 0x3: SDA0 0x4: SPI0_MISO 0x5: CCP1A 0x6: EPWM3 0x7: CTS1 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.20 P07 configuration register (IOP07CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP07CFG	P07 feature selection 0x0: GPIO 0x1: AN5 0x2: - 0x3: SCL0 0x4: SPI0_CLK 0x5: CCP1B 0x6: EPWM4 0x7: - 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.21 P10 configuration register (IOP10CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP10CFG	P10 feature selection 0x0: GPIO 0x1: AN6 0x2: TXD0 0x3: - 0x4: - 0x5: CCP0A 0x6: EPWM1 0x7: CTS1 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.22 P12 configuration register (IOP12CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP12CFG	P12 feature selection 0x0: GPIO 0x1: AN7/A1P0 0x2: RXD0 0x3: SDA0 0x4: SPI0_CLK 0x5: CCP1B 0x6: EPWM0 0x7: RTS1 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.23 P13 configuration register (IOP13CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP13CFG	P13 feature selection 0x0: GPIO/ECAP00 0x1: AN8/C0P0 0x2: TXD0 0x3: SCL0 0x4: SPI0_MISO 0x5: CCP1A 0x6: EPWM1 0x7: - 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.24 P14 configuration register (IOP14CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP14CFG	P14 feature selection 0x0: GPIO/ECAP01 0x1: AN9/C0P1 0x2: - 0x3: SDA0 0x4: SPI0_MOSI 0x5: CCP0A 0x6: EPWM4 0x7: - 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.25 P15 configuration register (IOP15CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP15CFG	P15 feature selection 0x0: GPIO/ECAP02 0x1: AN10/C0P2/A1P1 0x2: - 0x3: SCL0 0x4: SPI0_SS 0x5: CCP0A 0x6: EPWM5 0x7: - 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.26 P16 configuration register (IOP16CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP16CFG	P16 feature selection 0x0: GPIO 0x1: - 0x2: RXD0 0x3: SCL0 0x4: CTS0 0x5: CCP0B 0x6: EPWM2 0x7: AN11/OP1_O 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.27 P17 configuration register (IOP17CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP17CFG	P17 feature selection 0x0: GPIO 0x1: AN12/OP1_N 0x2: TXD0 0x3: SDA0 0x4: RTS0 0x5: CCP1A 0x6: EPWM4 0x7: - 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.28 P21 configuration register (IOP21CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP21CFG	P21 feature selection 0x0: GPIO 0x1: AN13/OP1_P 0x2: RXD0 0x3: SCL0 0x4: - 0x5: CCP1B 0x6: EPWM5 0x7: - 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.29 P22 configuration register (IOP22CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP22CFG	P22 feature selection 0x0: GPIO 0x1: AN14 0x2: TXD0 0x3: SCL0 0x4: CTS1 0x5: CCP0A 0x6: EPWM0 0x7: SDA0 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.30 P23 configuration register (IOP23CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP23CFG	P23 feature selection 0x0: GPIO 0x1: AN15/OP0_O 0x2: - 0x3: SDA0 0x4: RTS1 0x5: CCP0B 0x6: EPWM1 0x7: - 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.31 P24 configuration register (IOP24CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP24CFG	P24 feature selection 0x0: GPIO 0x1: AN16/OP0_N 0x2: - 0x3: SDA0 0x4: - 0x5: CCP1A 0x6: EPWM2 0x7: - 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.32 P25 configuration register (IOP25CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP25CFG	P25 feature selection 0x0: GPIO 0x1: AN17/OP0_P 0x2: - 0x3: SCL0 0x4: SPI0_SS 0x5: CCP1B 0x6: EPWM3 0x7: C1_O 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.33 P26 configuration register (IOP26CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP26CFG	P26 feature selection 0x0: GPIO 0x1: AN18 0x2: - 0x3: - 0x4: SPI0_CLK 0x5: CCP0A 0x6: EPWM4 0x7: C0_O 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.34 P30 configuration register (IOP30CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP30CFG	P30 feature selection 0x0: GPIO/ECAP13 0x1: AN19/C1P3/A1P2 0x2: RXD0 0x3: - 0x4: SPI0_CLK 0x5: CCP0B 0x6: EPWM0 0x7: ADET 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.35 P31 configuration register (IOP31CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP31CFG	P31 feature selection 0x0: GPIO/ECAP10 0x1: AN20/C1P0/A0P2 0x2: CTS0 0x3: SCL0 0x4: SPI0_MISO 0x5: CCP1A 0x6: EPWM4 0x7: - 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.36 P32 configuration register (IOP32CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP32CFG	P32 feature selection 0x0: GPIO/ECAP11 0x1: AN21/C1P1/A0P1 0x2: RXD0 0x3: SDA0 0x4: SPI0_MOSI 0x5: CCP1B 0x6: EPWM1 0x7: - 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.37 P34 configuration register (IOP34CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP34CFG	P34 feature selection 0x0: GPIO/ECAP12 0x1: AN22/C1P2/A0O 0x2: TXD0 0x3: SDA0 0x4: SPI0_CLK 0x5: CCP0A 0x6: EPWM3 0x7: - 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.38 P35 configuration register (IOP35CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP35CFG	P35 feature selection 0x0: GPIO 0x1: AN23/C1N/A1O 0x2: RTS0 0x3: SCL0 0x4: SPI0_SS 0x5: CCP0B 0x6: EPWM5 0x7: CLKO 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.39 P36 configuration register (IOP36CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP36CFG	P36 feature selection 0x0: GPIO/ECAP03 0x1: AN24/C0P3/A0P0 0x2: - 0x3: - 0x4: CLKO 0x5: CCP1A 0x6: EPWM0 0x7: -	0x0

		0x8: TXD1 0x9: RXD1 Other: Reserved	

2.5.3.40 P40 configuration register (IOP40CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP40CFG	P40 feature selection 0x0: GPIO 0x1: AN25 0x2: - 0x3: - 0x4: - 0x5: CCP1B 0x6: EPWM1 0x7: - 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.41 P43 configuration register (IOP43CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP43CFG	P43 feature selection 0x0: GPIO 0x1: AN26/C0N/A0P3 0x2: - 0x3: - 0x4: - 0x5: CCP0A 0x6: EPWM2 0x7: - 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.42 P44 configuration register (IOP44CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP44CFG	P44 feature selection 0x0: GPIO 0x1: AN27/A1P3 0x2: TXD0 0x3: - 0x4: - 0x5: CCP0B 0x6: EPWM1 0x7: -	0x0

		0x8: TXD1 0x9: RXD1 Other: Reserved	

2.5.3.43 P46 configuration register (IOP46CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP46CFG	P46 feature selection 0x0: GPIO 0x1: AN28 0x2: - 0x3: - 0x4: SPI0_MISO 0x5: CCP1A 0x6: EPWM2 0x7: SWDCLK0 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.44 P47 configuration register (IOP47CFG)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3:0	IOP47CFG	P47 feature selection 0x0: GPIO 0x1: AN29 0x2: - 0x3: RTS1 0x4: SPI0_MOSI 0x5: CCP1B 0x6: EPWM5 0x7: SWDDAT0 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

2.5.3.45 System detection interrupt enable register (SYS_IMSC)

Bit	Symbol	Description	Reset value
31:5	-	Reserved	-
4	LVD_IMSC	LVD interrupt enable bit 0: Disable 1: Enable	0x0
3:0	-	Reserved	-

2.5.3.46 System detection interrupt source status register (SYS_RIS)

Bit	Symbol	Description	Reset value
31:5	-	Reserved	-
4	LVD_RIS	LVD interrupt source status 0: The VDD voltage is higher than the set voltage (no interrupts are generated or the interrupts are cleared). 1: The VDD voltage is lower than the set voltage (generating an interrupt).	0x0
3:0	-	Reserved	-

2.5.3.47 System detection enabled interrupt status register (SYS_MIS)

Bit	Symbol	Description	Reset value
31:5	-	Reserved	-
4	LVD_MIS	LVD interrupt status 0: No interrupt generated 1: Enabled and produced an interrupt	0x0
3:0	-	Reserved	-

2.5.3.48 System detection interrupt clear register (SYS_ICLR)

Bit	Symbol	Description	Reset value
31:5	-	Reserved	-
4	LVD_ICLR	Write 1 to clear LVD interrupt status Writing 0 does not affect	0x0
3:0	-	Reserved	-

2.5.3.49 Internal oscillation frequency trimming register (HSI_TRIM)

Bit	Symbol	Description	Reset value
31:16	-	Write 0x5A69 at the same time to operate on the other bits of this register.	0x0
15:8	-	Reserved	-
7:0	TRIM	Internal oscillation frequency trimming bit When powering up or changing the CLKCON [0] bit, the system automatically loads the factory trimming value	-

2.5.3.50 SRAM write enable register (SRAMLOCK)

Bit	Symbol	Description	Reset value
31:8	LOCK	When LOCK=0x55AA, the protection function of SRAM takes effect	0x0
7:4	-	Reserved	-
3:0	REGION	Bit3: Set SRAM address 0x20001800-0x20001FFF area to write-protected state Bit2: Set SRAM address 0x20001000-0x200017FF area to write-protected state Bit1: Set SRAM address 0x20000800-0x20000FFF area to write-protected state Bit0: --- When writing 0, the protection function is disabled. (R/W) When writing 1, the protection function is enabled. () Note: The 2KBytes area with an initial address range of 0x20000000-0x200007FF is free to read and write.	0x0

2.5.3.51 GPIO0 write enable register (GPIO0LOCK)

Bit	Symbol	Description	Reset value
31:0	LOCK	When LOCK=0x99, enables GPIO0 related register to read the value of 0x99 When LOCK= other values, operation of the GPIO0-related registers is prohibited	0x0

2.5.3.52 GPIO1 write enable register (GPIO1LOCK)

Bit	Symbol	Description	Reset value
31:0	LOCK	When LOCK=0x99, enables GPIO1 related register to read the value of 0x99 When LOCK= other values, operation of the GPIO1-related registers is prohibited	0x0

2.5.3.53 GPIO2 write enable register (GPIO2LOCK)

Bit	Symbol	Description	Reset value
31:0	LOCK	When LOCK=0x99, enables GPIO2 related register to read the value of 0x99 When LOCK= other values, operation of the GPIO2-related registers is prohibited	0x0

2.5.3.54 GPIO3 write enable register (GPIO3LOCK)

Bit	Symbol	Description	Reset value
31:0	LOCK	When LOCK=0x99, enables GPIO3 related register to read the value of 0x99 When LOCK= other values, operation of the GPIO3-related registers is prohibited	0x0

2.5.3.55 GPIO4 write enable register (GPIO4LOCK)

Bit	Symbol	Description	Reset value
31:0	LOCK	When LOCK=0x99, enables GPIO4 related register to read the value of 0x99 When LOCK= other values, operation of the GPIO4-related registers is prohibited	0x0

2.5.3.56 Port configuration write enable register (IOCFGLOCK)

Bit	Symbol	Description	Reset value
31:0	IOCFGLOCK	When LOCK=0x99, enable the operation of port configuration related registers, the read value is 0x99. When LOCK=0x99, enable operation of port configuration related registers, the read value is 0x99.	0x0

2.6 System Timer (SysTick)

The Cortex®M0 has a built-in system timer, the SysTick, which provides a simple 24-bit write clear, decrement counting, and auto-load initial value function, as well as a register with a flexible control mechanism. The counter can be used as a real-time operating system (RTOS) tick timer or as a simple timer peripheral.

When the system timer is enabled, the value of the SysTick current value register (SysTickVAL) is counted down to 0, and at the next clock edge, the value of the SysTick reload value register (SysTickLOAD) is reloaded, and then decremented at any time. When the counter is decremented to 0, the COUNTFLAG status bit is set to 1 and the SysTickCTRL register is read to clear the COUNTFLAG bit.

The clock source for the system timer is the system clock (SCLK).

Note: When the kernel is in a suspended state, the count stops decrementing.

2.6.1 Register mapping

(SysTick base address = 0Xe000_E010) RO: read only; WO: write only; R/W: read and write.

Register	Offset value	R/W	Description	Reset value
SysTickCTRL	0x000	R/W	SysTick control and status register	0x0
SysTickLOAD	0x004	R/W	SysTick reload value register	-
SysTickVAL	0x008	R/W	SysTick current value register	-
SysTickCALIB	0x00C	RO	SysTick calibration value register	0x40028B0A

2.6.2 Register description

2.6.2.1 SysTick control and status register (SysTickCTRL)

Bit	Symbol	Description	Reset value
31:17	-	Reserved	-
16	COUNTFLAG	When the SysTick counter decrements the count to 0, the bit is set, read the register will clear the bit.	0x0
15:2	-	Reserved	-
1	INT	SysTick interrupt enable bit 0: Disable SysTick Interrupt 1: Enable SysTick interrupt	0x0
0	EN	SysTick counter enable bit 0: Disable 1: Enable	0x0

2.6.2.2 SysTick reload register (SysTickLOAD)

Bit	Symbol	Description	Reset value
31:24	-	Reserved	-
23:0	RELOAD	When the counter is enabled and counts to 0, the value is reloaded into the SysTickVAL register.	-

2.6.2.3 SysTick current value register (SysTickVAL)

Bit	Symbol	Description	Reset value
31:24	-	Reserved	-
23:0	CURRENT	The current value of the SysTick counter is returned when the register is read; Write any data to clear the SysTick counter while clearing the COUNTFLAG bit in the SysTickCTRL register.	-

2.6.2.4 SysTick calibration value register (SysTickCALIB)

Bit	Symbol	Description	Reset value
31	-	Reserved	-
30	SKEW	Displays whether the TENMS value is accurate or not, an inaccurate TENMS value will affect how well the SysTick matches as a software real-time clock. 0: The TENMS value is accurate; 1: The TENMS value is inaccurate or non-existent.	0x0
29:24	-	Reserved	-
23:0	TENMS	This is a reloaded value for the 10ms timing effect, and is also affected by system clock offset. If this value reads 0, then this calibration value is undefied.	0x000004

2.7 Nested vector interrupt controller (NVIC)

The Cortex-M0® CPU provides a nested vector interrupt controller (NVIC) for interrupt handling.

2.7.1 Features

- Nested vector interrupts are supported.
- Automatically save and restore processor state.
- Dynamically change priorities.
- Simplify and determine interrupt times.

The NVIC handles all supported exceptions in priority. All exceptions are handled in “Handler mode”. The NVIC supports 32 (IRQ[31:0]) discrete interrupts, each with 4 levels of interrupt priority. All Interrupts and most system exceptions can be configured with different priorities. When an interrupt occurs, the NVIC will prioritize the new interrupt against the current interrupt, and if the new interrupt has a high priority, the new interrupt will be processed immediately.

When an interrupt is accepted, the start address of the interrupt service program (ISR) is available from the in-memory vector table. The software does not need to decide which interrupt is responded to, nor does it need to assign the start address of the relevant ISR. When the start address is obtained, the NVIC automatically saves the processor status registers (PC, PSR, LR, R0~R3, R12) to the stack. After the ISR ends, the NVIC will recover the values of the relevant registers from the stack and run in a normal state. So, it takes a small and certain amount of time to process the interrupt request.

The NVIC supports “end-to-end chaining” that can effectively handle back-to-back interrupts, i.e. without saving and restoring the current state, thereby reducing the delay in completing the current ISR to switching to a pending ISR. The NVIC also supports “Late Arrival”, so it can improve the efficiency of concurrent interrupts. When a higher priority interrupt request occurs before the current ISR starts executing (the stage of saving the processor state and getting the start address), the NVIC will immediately process the higher priority interrupt, improving real-time.

For more details, please refer to the ARM®Cortex-M0® Technical Reference Manual and the ARM®v6-M Architecture Reference Manual.

2.7.2 Exception mode and system interrupt mapping

The following table lists the exception mode supported by the CMS32F033 series. As with all interrupts, the software can set up to 4 priority levels for some of these exceptions. The highest user-configurable priority is 0, and the lowest priority is 3. The default priority for all user-configurable interrupts is 0.

Exception name	Exception number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4~10	Reserved
SVCall	11	Configurable
Reserved	12~13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0~IRQ31)	16~47	Configurable

Note: Priority 0 is the fourth priority in the system, after “Reset”, “NMI” and “Hard Fault”.

2.7.3 Vector table

Exception number	Interrupt	Vector address	Exception type	description
1-15	-	0x00-0x3c	System exception	
16	0	0x40	GPIO0	P0[7:0] interrupt
17	1	0x44	GPIO1	P1[7:0] interrupt
18	2	0x48	GPIO2	P2[7:0] interrupt
19	3	0x4c	GPIO3	P3[7:0] interrupt
20	4	0x50	GPIO4	P4[7:0] interrupt
21	5	0x54	-	-
22	6	0x58	CCP	Capture/PWM interrupt
23	7	0x5c	-	-
24	8	0x60	-	-
25	9	0x64	WWDT	WWDT interrupt
26	10	0x68	EPWM	EPWM interrupt
27	11	0x6c		
28	12	0x70	ADC1	ADC1 interrupt
29	13	0x74	ACMP	ACMP interrupt
30	14	0x78	-	
31	15	0x7c	UART0	UART0 interrupt
32	16	0x80	UART1	UART1 interrupt
33	17	0x84	-	
34	18	0x88	-	-
35	19	0x8c	TIMER0	Timer0 interrupt
36	20	0x90	TIMER1	Timer1 interrupt
37	21	0x94	-	
38	22	0x98	-	-
39	23	0x9c	WDT	Watchdog interrupt
40	24	0xa0	I2C	I2C interrupt
41	25	0xa4	-	-
42	26	0xa8	SSP/SPI	SSP/SPI interrupt
43	27	0xac	-	
44	28	0xb0	-	
45	29	0xb4	-	
46	30	0xb8	-	-
47	31	0xbc	SYS_CHK	System detection interrupt (LVD interrupt)

2.7.4 Register mapping

(NVIC base address = 0Xe000_E000) RO: read only; WO: write only; R/W: read and write.

Register	Offset value	R/W	Description	Reset value
ISER	0x100	R/W	Interrupt set enable control register	0x0
ICER	0x180	R/W	Interrupt clear enable control register	0x0
ISPR	0x200	R/W	Interrupt set pending control register	0x0
ICPR	0x280	R/W	Interrupt clear pending control register	0x0
IPR0	0x400	R/W	IRQ0~IRQ3 interrupt priority register	0x0
IPR1	0x404	R/W	IRQ4~IRQ7 interrupt priority register	0x0
IPR2	0x408	R/W	IRQ8~IRQ11 interrupt priority register	0x0
IPR3	0x40C	R/W	IRQ12~IRQ15 interrupt priority register	0x0
IPR4	0x410	R/W	IRQ16~IRQ19 interrupt priority register	0x0
IPR5	0x414	R/W	IRQ20~IRQ23 interrupt priority register	0x0
IPR6	0x418	R/W	IRQ24~IRQ27 interrupt priority register	0x0
IPR7	0x41C	R/W	IRQ28~IRQ31 interrupt priority register	0x0

2.7.5 Register description

2.7.5.1 Interrupt set enable control register (ISER)

Bit	Symbol	Description	Reset value
31:0	SETENA	Interrupt enable bit Enable one or more interrupts. Each bit represents an interrupt from IRQ0 to IRQ31 (Vector number from 16 to 47). Write: 0: Invalid 1: Write 1 to enable the relevant interrupt Read: 0: The relevant interrupt status is prohibited 1: The relevant interrupt state is enabled Note: Reading the register value indicates the current enable state.	0x0

2.7.5.2 Interrupt clear enable control register (ICER)

Bit	Symbol	Description	Reset value
31:0	CLRENA	Interrupt disable bit Disable one or more interrupts. Each bit represents an interrupt from IRQ0 to IRQ31(Vector number from 16 to 47). Write: 0: Invalid 1: Write 1 to enable the relevant interrupt Read: 0: The relevant interrupt status is prohibited 1: The relevant interrupt state is enabled Note: Reading the register value indicates the current enable state.	0x0

2.7.5.3 Interrupt set pending control register (ISPR)

Bit	Symbol	Description	Reset value
31:0	SETPEND	Set the interrupt pending bi Write: 0: Invalid 1: Write 1 to set the pending state. Each bit represents an interrupt from IRQ0 to IRQ31 (vector number from 16 to 47). Read: 0: The related interrupt is not in the pending state 1: The related interrupt is in the pending state Note: Reading the register value indicates the current pending state.	0x0

2.7.5.4 Interrupt clear pending control register (ICPR)

Bit	Symbol	Description	Reset value
31:0	CLRPEND	Clear interrupt pending bit Write: 0: Invalid 1: Write 1 to clear the pending state. Each bit represents an interrupt from IRQ0 to IRQ31 (vector number from 16 to 47). Read: 0: The related interrupt is not in the pending state 1: The related interrupt is in the pending state Note: Reading the register value indicates the current pending state.	0x0

2.7.5.5 IRQ0~IRQ3 interrupt priority register (IPR0)

Bit	Symbol	Description	Reset value
31:30	PRI_3	IRQ3 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
29:24	-	Reserved	-
23:22	PRI_2	IRQ2 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
21:16	-	Reserved	-
15:14	PRI_1	IRQ1 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
13:8	-	Reserved	-
7:6	PRI_0	IRQ0 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
5:0	-	Reserved	-

2.7.5.6 IRQ4~IRQ7 interrupt priority register (IPR1)

Bit	Symbol	Description	Reset value
31:30	PRI_7	IRQ7 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
29:24	-	Reserved	-
23:22	PRI_6	IRQ6 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
21:16	-	Reserved	-
15:14	PRI_5	IRQ5 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
13:8	-	Reserved	-
7:6	PRI_4	IRQ4 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
5:0	-	Reserved	-

2.7.5.7 IRQ8~IRQ11 interrupt priority register (IPR2)

Bit	Symbol	Description	Reset value
31:30	PRI_11	IRQ11 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
29:24	-	Reserved	-
23:22	PRI_10	IRQ10 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
21:16	-	Reserved	-
15:14	PRI_9	IRQ9 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
13:8	-	Reserved	-
7:6	PRI_8	IRQ8 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
5:0	-	Reserved	-

2.7.5.8 IRQ12~IRQ15 interrupt priority register (IPR3)

Bit	Symbol	Description	Reset value
31:30	PRI_15	IRQ15 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
29:24	-	Reserved	-
23:22	PRI_14	IRQ14 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
21:16	-	Reserved	-
15:14	PRI_13	IRQ13 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
13:8	-	Reserved	-
7:6	PRI_12	IRQ12 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
5:0	-	Reserved	-

2.7.5.9 IRQ16~IRQ19 interrupt priority register (IPR4)

Bit	Symbol	Description	Reset value
31:30	PRI_19	IRQ19 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
29:24	-	Reserved	-
23:22	PRI_18	IRQ18 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
21:16	-	Reserved	-
15:14	PRI_17	IRQ17 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
13:8	-	Reserved	-
7:6	PRI_16	IRQ16 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
5:0	-	Reserved	-

2.7.5.10 IRQ20~IRQ23 interrupt priority register (IPR5)

Bit	Symbol	Description	Reset value
31:30	PRI_23	IRQ23 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
29:24	-	Reserved	-
23:22	PRI_22	IRQ22 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
21:16	-	Reserved	-
15:14	PRI_21	IRQ21 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
13:8	-	Reserved	-
7:6	PRI_20	IRQ20 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
5:0	-	Reserved	-

2.7.5.11 IRQ24~IRQ27 interrupt priority register (IPR6)

Bit	Symbol	Description	Reset value
31:30	PRI_27	IRQ27 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
29:24	-	Reserved	-
23:22	PRI_26	IRQ26 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
21:16	-	Reserved	-
15:14	PRI_25	IRQ25 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
13:8	-	Reserved	-
7:6	PRI_24	IRQ24 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
5:0	-	Reserved	-

2.7.5.12 IRQ28~IRQ31 interrupt priority register (IPR7)

Bit	Symbol	Description	Reset value
31:30	PRI_31	IRQ31 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
29:24	-	Reserved	-
23:22	PRI_30	IRQ30 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
21:16	-	Reserved	-
15:14	PRI_29	IRQ29 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
13:8	-	Reserved	-
7:6	PRI_28	IRQ28 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
5:0	-	Reserved	-

2.8 System control block (SCB)

The status and operating mode of the Cortex-M0® are managed by the System Control Block. The CPUID, Cortex®-M0 interrupt priority, and Cortex®-M0 power management can be controlled through the relevant registers of the system control block.

For more details, please refer to the "ARM®Cortex-M0® Technical Reference Manual" and the "ARM®v6-M Architecture Reference Manual".

2.8.1 Register mapping

(SCB base address = 0Xe000_ED00) RO: read only; WO: write only; R/W: read and write.

Register	Offset value	R/W	Description	Reset value
CPUID	0x000	RO	CPUID register	0x410CC200
ICSR	0x004	R/W	Interrupt control status register	0x0
AIRCR	0x00C	R/W	Apply interrupt and reset control register	0Xfa050000
SCR	0x010	R/W	System control register	0x0
SHPR2	0x01C	R/W	System handling priority register 2	0x0
SHPR3	0x020	R/W	System handling priority register 3	0x0

2.8.2 Register description

2.8.2.1 CPUID register (CPUID)

Bit	Symbol	Description	Reset value
31:24	Implementer	Execute the code =0x41, assigned by ARM	0x41
23:20	Variant	Version number 0x0	0x0
19:16	Constant	Processor architecture =0Xc, which represents the ARMv6-M architecture	0Xc
15:4	Partno	Processor product number =0Xc20, which represents the Cortex-M0	0Xc20
3:0	Revision	Revision number 0x0	0x0

2.8.2.2 Interrupt control status register (ICSR)

Bit	Symbol	Description	Reset value
31	NMIPENDSET	NMI set pending bit Write: 0= Invalid 1= Set NMI exception pending Read: 0= NMI exception is not pending 1= NMI exception is pending Note: Since NMI is the highest priority exception, the processor normally enters an NMI exception as soon as it detects a write of 1 to this bit. After entering the exception, the processor will clear the bit to zero. This means that only when the processor is executing the NMI exception handler, and the NMI signal is generated again, the NMI exception handler reads this bit and returns 1.	0x0
30:29	-	Reserved	-
28	PENDSVSET	PendSV set pending bit Write: 0= Invalid 1= Set PendSV exception pending Read: 0= PendSV is not pending 1= PendSV is pending Note: Setting this bit to 1 is the only way to set pending PendSV exceptions.	0x0
27	PENDSVCLR	PendSV clear pending bit Write: 0= Invalid 1= Clears the PendSV exception pending state Note: This bit is a write-only bit. In order to clear the PENDSV bit, you must also write 0 to PENDSVSET and 1 to PENDSVCLR.	0x0
26	PENDSTSET	SysTick exception set pending bit Write: 0= Invalid 1= Set SysTick exception pending Read: 0= SysTick is not pending 1= SysTick is pending	0x0
25	PENDSTCLR	SysTick exception clear pending bit Write: 0= Invalid 1= Clear SysTick exception pending status Note: This bit is read-only. When you want to clear the PENDST bit, you must write 0 to PENDSTSET and 1 to PENDSTCLR at the same time.	0x0
24	-	Reserved	-
23	ISRPREEMPT	Interrupt preemptive occupied bit If this bit set to 1, a pending exception exits from the debug stop state and enters exception handling. Note: This bit is read-only	0x0
22	ISRPENDING	Interrupt pending flag (excluding NMI and Faults) 0= The interrupt is not pending 1= The interrupt is pending Note: This bit is read-only	0x0
21	-	Reserved	-
20:12	VECTPENDING	The highest priority exception number among pending exceptions 0= No exception is pending Other than 0= The highest priority exception number among pending exceptions is pending Note: This bit is read-only	0x0
11:9	-	Reserved	-
8:0	VECTACTIVE	Include the current exception number	0x0

		0= Thread mdoe Other than 0= Current executing exception number Note: These bits are read-only	

2.8.2.3 Apply interrupt and reset control register (AIRCR)

Bit	Symbol	Description	Reset value
31:16	VECTORKEY	Register access key Write: - When writing this register, the VECTORKEY bit field must be set to 0x05FA, otherwise writes will be ignored. - The VECTORKEY bit field is used to prevent the register from being written incorrectly when the system resets or clears the abnormal state. Read: The value read out is 0xFA05	0Xfa05
15	ENDIANESS	The endianess format of the memory Read only 0= Little-endian 1= Big-endian	0x0
14:3	-	Reserved	-
2	SYSRESETREQ	System reset request Writing 1 to this bit will cause a reset signal to the chip, indicating that there is a reset request. This bit is a write-only bit, and it is automatically cleared to zero after reset.	0x0
1	VECTCLRACTIVE	Exception valid status clear bit Reserved for debugging use. When writing this register, the user must write 0 to that bit, otherwise unpredictable situations will occur.	0x0
0	-	Reserved	-

2.8.2.4 System control register (SCR)

Bit	Symbol	Description	Reset value
31:5	-	Reserved	-
4	SEVONPEND	Transmit an event when pending 0= Only enable interrupts or events can wake up the processor, excluding disabled interrupts. 1= Enable events and all interrupts, including disabled interrupts, to wake up the processor. When an event or interrupt enters a pending state, the event signal wakes the processor from the WFE. If the processor is not waiting for an event, the event will be registered and affect the next WFE. Executing SEV instructions or external events also wakes up the processor.	0x0
3:2	-	Reserved, set to 0.	-
1	SLEEPONEXIT	Sleep-On-Exit enabled This bit indicates whether to exit sleep when returning to Thread mode from Handler mode 0= When returned from thread mode, it does not sleep 1= When returning to Thread mode from the ISR, go into hibernation or deep sleep This bit set to 1 enables an interrupt-driven application, thus avoiding returning to an empty main function application.	0x0
0	-	Reserved	-

2.8.2.5 System handling priority register 2 (SHPR2)

Bit	Symbol	Description	Reset value
31:30	PRI_11	System Exception Number 11 – Priority of SVCall 0: Highest priority 3: Lowest priority	0x0
29:0	-	Reserved	-

2.8.2.6 System handling priority register 3 (SHPR3)

Bit	Symbol	Description	Reset value
31:30	PRI_15	System exception number 15 – Priority of SysTick 0: Highest priority 3: Lowest priority	0x0
29:24	-	Reserved	-
23:22	PRI_14	System exception number 14 – Priority of PendSV 0: Highest priority 3: Lowest priority	0x0
21:0	-	Reserved	-

2.9 User Configuration

2.9.1 Overview

The user configuration area is a 128-word storage area allocated in FLASH, which is a system reserved register for configuring external reset IO multiplexing function, encryption function, user ID and other information.

2.9.2 Register mapping

(Base address = 0x1000_0000) RO: read only; WO: write only; R/W: read and write.

Register	Offset value	R/W	Description	Reset value
Config0	0x000	RO	User configuration register0	-
Config1	0x004	RO	User configuration register1	-
Config2	0x010	RO	User configuration register2	-
Config3	0x014	RO	User configuration register3	-
USRUID0	0x024	RO	User unique chip identification number ID0	-
USRUID1	0x028	RO	User unique chip identification number ID1	-
USRUID2	0x02c	RO	User unique chip identification number ID2	-

2.9.3 Register description

2.9.3.1 User configuration register0 (Config0)

Bit	Symbol	Description	Reset value
31:13	-	Reserved	-
12:11	Reset voltage selection bit	Reset voltage selection bit 10: 2.6V 01: 2.1V 00: 1.9V	-
10:8	-	Reserved	-
7:4	BOOT_TYPE	Program start position selection on power-on reset (requires allocation of valid BOOT space). 1111: - 0011: Boot from APROM 0001: Boot from the BOOT area 0000: Start from the BOOT area, configure the BOOT pin as a dedicated port, and require the BOOT pin = 0 Other: Boot from APROM Note: Booting from theBOOT area requires allocating a valid BOOT space, otherwise booting from APROM	-
3	-	Set to 0	-
2	USRIDPE	User UID encryption bit 1: Not encrypted 0: Encrypted	-
1	-	Set to 1	-
0	DATA-PROTECT	Encryption bit 1: Not encrypted 0: Encrypted	-

2.9.3.2 User configuration register 1 (Config1)

Bit	Symbol	Description	Reset value
31:28	CONFIG_EN_WDT	WDT enable bit 1111: Power-on does not enable WDT Other: Power-on enables WDT	-
27:24	WDT_TIME	0000: 2ms (WDTLOAD=0x50) 0001: 4ms (WDTLOAD=0Xa0) 0010: 8ms (WDTLOAD=0x140) 0011: 16ms (WDTLOAD=0x280) 0100: 32ms (WDTLOAD=0x500) 0101: 64ms (WDTLOAD=0Xa00) 0110: 128ms (WDTLOAD=0x1400) 0111: 256ms (WDTLOAD=0x2800) 1000: 512ms (WDTLOAD=0x5000) 1001: 1024ms (WDTLOAD=0Xa000) 1010: 1638ms (WDTLOAD=0Xffff) 1011: 1638ms (WDTLOAD=0Xffff) 1100: 1638ms (WDTLOAD=0Xffff) 1101: 1638ms (WDTLOAD=0Xffff) 1110: 1638ms (WDTLOAD=0Xffff) 1111: 1638ms (WDTLOAD=0Xffff)	-
23:14	-	Reserved	-
13:12	DEBUGEN	SWD debug enable bit 00: Disable Other: Enable	-
11:10	RESETIOS	External reset selection 11: External reset disabled 10: P10 acts as an external reset port 01: P44 acts as an external reset port 00: P43 acts as an external reset port	-
9:0	-	Reserved	-

2.9.3.3 User configuration register 2 (Config2)

Bit	Symbol	Description	Reset value
31:16	-	Reserved	-
15:0	USRAPE	APROM program space write-protect bit (every 2K) If BOOT area is allocated, Bit14, Bit15 act on valid APROM area. The protection status is: SWD prohibits read/write/single page erase. Normal operation prohibits write/erase. BOOT program operation is not affected Bit0: 0x0000-0x07FF (Absolute address of FLASH) Bit1: 0x0800-0x0FFF Bit2: 0x1000-0x17FF …… Bit14: 0x7000-0x77FF Bit15: 0x7800-0x7FFF 0: Protected 1: Not protected	-

2.9.3.4 User configuration register 3 (Config3)

Bit	Symbol	Description	Reset value
31:20	-	Reserved	-
19:16	USRBTS	APROM/BOOTspace allocation bit 0000: APROM=28K; BOOT=4K 0001: APROM=30K; BOOT=2K 0010: APROM=31K; BOOT=1K Other: APROM=32K; BOOT=0K	-
15:4	-	-	-
3:0	USRBPE	BOOT program space write protect bit (every 1K) If the BOOT area is less than 4K, the protection bit acts on the valid BOOT area. The protection status is. SWD prohibits read/write/single page erase. Normal operation prohibits read/write/erase. BOOT program disables read/write/erase. Bit0: 0x7000-0x73FF (Absolute address of FLASH) Bit1: 0x7400-0x77FF Bit2: 0x7800-0x7BFF Bit3: 0x7C00-0x7FFF 0: Protected 1: Not protected	-

2.9.3.5 User unique identification number ID0 (USRUID0)

Bit	Symbol	Description	Reset value
31:0	USRUID0	Bits [31:0] of the user unique chip identification number ID	-

2.9.3.6 User unique identification number ID1 (USRUID1)

Bit	Symbol	Description	Reset value
31:0	USRUID1	Bits [63:32] of the user unique chip identification number ID	-

2.9.3.7 User unique identification number ID2 (USRUID2)

Bit	Symbol	Description	Reset value
31:0	USRUID2	Bits [95:64] of the user unique chip identification number ID	-

3. Feature Description

3.1 General I/O (GPIO)

3.1.1 Overview

Up to 30 general-purpose I/O pins, each I/O port can be configured by software into a normal input, pull-up input, pull-down input, push-pull output, and no pull-out leakage output mode. These pins can be shared by configuring the chip and other functional pins.

3.1.2 Features

- Five I/O modes.
  - Normal input.
  - Pull-up input.
  - Pull-down input.
  - Push-pull output.
  - Open-drain output without pull-up.
- I/O can be configured to trigger interrupts at edges/levels.
- 2-stage output current configuration.
- 2-stage I/O speed configuration.

3.1.3 Feature description

3.1.3.1 Input mode

Set GPIOxPMS [4n+2:4n] to 000, Px.n pins to input mode, I/O pins to high-impedance state, no drive capability.

3.1.3.2 Pull-up input mode

Set GPIOxPMS [4n+2:4n] to 001, Px.n pins to pull-up input mode, and I/O pins to internally connect pull-up resistors.

3.1.3.3 Pull-down input mode

Set GPIOxPMS [4n+2:4n] to 100, Px.n pins to pull-down input mode, and I/O pins to internally connect pull-down resistors.

3.1.3.4 Push-pull output mode

Set GPIOxPMS [4n+2:4n] to 001, Px.n pins to push-pull output mode, and I/O support digital output function with source/sink current capability. The value of the DO corresponding bit[n] is sent to the corresponding pin.

3.1.3.5 Open-drain output without pull-up

Set GPIOxPMS [4n+2:4n] to 010, Px.n pins to open-drain output mode, I/O pin digital output function only supports current sinking, and pull resistors are required to drive high. If the DO corresponding bit is '0', the output is low on the pins. If the DO corresponding bit is '1', the pin is set high by an external pull-up resistor.

3.1.3.6 Interrupt and wake-up function

Each GPIO pin can be set as the interrupt source of the chip. There are five types of interrupt triggering conditions that can be set: low level trigger, high level trigger, falling edge trigger, rising edge trigger and both rising and falling edge trigger. In the edge trigger, users can enable the input signal de-jitter function to prevent unexpected interrupt caused by noise.

The GPIOs can also wake up the system when the chip enters sleep/deep sleep mode. The following are the conditions that need to be noted:

Falling edge wake-up requires the port level to be pulled high before entering the low-power state.

Rising edge wake-up requires the port level to be pulled low before entering the low-power state.

3.1.4 Register mapping

GPIO0 base address = 0x5200_0000;
GPIO1 base address = 0x5280_0000;
GPIO2 base address = 0x5300_0000;
GPIO3 base address = 0x5380_0000;
GPIO4 base address = 0x5400_0000;
RO: read only; WO: write only; R/W: read and write.
The x values in the following registers range from 0-5.

Register	Offset value	R/W	Description	Reset value
PMS(P1A)	0x000	R/W	GPIOx mode select register 1	0x0
DOM(P1A)	0x004	R/W	GPIOx data output write mask register 1	0x0
DO(P1A)	0x008	R/W	GPIOx data output register 1	0Xff
DI	0x00c	RO	GPIOx pin status data register	-
IMSC(P1A)	0x010	R/W	GPIOx interrupt enable register 1	0x0
RIS	0x014	RO	GPIOx interrupt source status register	0x0
MIS	0x018	RO	GPIOx enabled interrupt status register	0x0
ICLR(P1A)	0x01c	WO	GPIOx interrupt status clear register 1	0x0
ITYPE(P1A)	0x020	R/W	GPIOx interrupt trigger mode register 1	0x0
IVAL(P1A)	0x024	R/W	GPIOx interrupt trigger value register 1	0x0
IANY(P1A)	0x028	R/W	GPIOx interrupt edge trigger mode register 1	0x0
DIDB(P1A)	0x02c	R/W	GPIOx input filtering control register 1	0x0
DOSET(P1A)	0x030	WO	GPIOx output set register	0x0
DOCLR(P1A)	0x034	WO	GPIOx output clear register	0x0
DR(P1A)	0x038	R/W	GPIOx drive current set register 1	0Xff
SR(P1A)	0x03C	R/W	GPIOx output rate setting register 1	0Xff

Note:
(P1A) The registers marked are protected registers.
(P1A): When GPIOxLOCK=99H, the marked registers are allowed to write; = Other values, forbidden to write.
(GPIOxLOCK registers are shown in the system control section)

3.1.5 Register description

3.1.5.1 GPIOx mode selection register (GPIOxPMS)

Bit	Symbol	Description	Reset value
31	-	Reserved	-
30:28	PMS7	Px.7 mode selection 0x0: Normal input 0x1: Push-pull output 0x2: Open-drain output without pull-up 0x3: Pull-up input 0x4: Pull-down input Other value: Reserved	0x0
27	-	Reserved	-
26:24	PMS6	Px.6 mode selection 0x0: Normal input 0x1: Push-pull output 0x2: Open-drain output without pull-up 0x3: Pull-up input 0x4: Pull-down input Other value: Reserved	0x0
23	-	Reserved	-
22:20	PMS5	Px.5 mode selection 0x0: Normal input 0x1: Push-pull output 0x2: Open-drain output without pull-up 0x3: Pull-up input 0x4: Pull-down input Other value: Reserved	0x0
19	-	Reserved	-
18:16	PMS4	Px.4 mode selection 0x0: Normal input 0x1: Push-pull output 0x2: Open-drain output without pull-up 0x3: Pull-up input 0x4: Pull-down input Other value: Reserved	0x0
15	-	Reserved	-
14:12	PMS3	Px.3 mode selection 0x0: Normal input 0x1: Push-pull output 0x2: Open-drain output without pull-up 0x3: Pull-up input 0x4: Pull-down input Other value: Reserved	0x0
11	-	Reserved	-
10:8	PMS2	Px.2 mode selection 0x0: Normal input 0x1: Push-pull output 0x2: Open-drain output without pull-up 0x3: Pull-up input 0x4: Pull-down input Other value: Reserved	0x0
7	-	Reserved	-
6:4	PMS1	Px.1 mode selection 0x0: Normal input 0x1: Push-pull output 0x2: Open-drain output without pull-up 0x3: Pull-up input 0x4: Pull-down input	0x0

		Other value: Reserved	
3	-	Reserved	-
2:0	PMS0	Px.0 mode selection 0x0: Normal input 0x1: Push-pull output 0x2: Open-drain output without pull-up 0x3: Pull-up input 0x4: Pull-down input Other value: Reserved	0x0

3.1.5.2 GPIOx data output write mask register (GPIOxDOM)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	DOM	Px[7:0] data output write mask bit 1: This bit data of DO register is not writable 0: This bit data of DO register is writable	0x0

3.1.5.3 GPIOx data output register (GPIOxDO)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	DO	Px[7:0] output value 1: Output high 0: Output low	0xff

3.1.5.4 GPIOx pin status register (GPIOxDI)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	DI	Pin status input data	-

3.1.5.5 GPIOx interrupt enable register (GPIOxIMSC)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	IMSC	Px[7:0] interrupt enable bit 1: Enable 0: Disable	0x0

3.1.5.6 GPIOx interrupt source status register (GPIOxRIS)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	RIS	Px[7:0] interrupt source status bit 1: An interrupt is generated on the pin. 0: An interrupt is not generated on the pin.	0x0

3.1.5.7 GPIOx enabled interrupt status register (GPIOxMIS)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	MIS	Px[7:0] enabled interrupt status bit 1: A pin interrupt is enabled and an interrupt is generated 0: No interrupt generated	0x0

3.1.5.8 GPIOx interrupt status clear register (GPIOxICLR)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	ICLR	Px[7:0] interrupt status clear bit Write 1, clear the corresponding bits of GPIOxRIS and GPIOxMIS.	0x0

3.1.5.9 GPIOx interrupt trigger mode selection register (GPIOxITYPE)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	ITYPE	Px[7:0] interrupt trigger mode select bit 0: Edge trigger 1: Level trigger	0x0

3.1.5.10 GPIOx interrupt trigger value register (GPIOxIVAL)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	IVAL	Px[7:0] interrupt/sleep wake trigger condition selection bit 0: Low-level trigger or falling edge trigger 1: High-level trigger or rising edge trigger	0x0

3.1.5.11 GPIOx interrupt edge trigger mode register (GPIOxIANY)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	IANY	Px[7:0] interrupt edge trigger mode select bit 0: Triggered by falling edge or rising edge, as determined by GPIOxIVAL registers 1: Triggered by both the rising and falling edges	0x0

3.1.5.12 GPIOx input filtering control register (GPIOxDIDB)

Bit	Symbol	Description	Reset value
31:11	-	Reserved	-
10:8	DBCKS	Px input filtering sampling clock selection bit 000: HCLK 001: HCLK/2 010: HCLK/4 011: HCLK/6 100: HCLK/8 101: HCLK/10 110: HCLK/12 111: HCLK/14	0x0
7:0	DIDB	Px[7:0] input filter enable bit 0: Pin level via Schmitt input directly to GPIOxDI and interrupt edge detection 1: After the pin level has gone through the Schmitt input it also needs to go through a filter circuit to GPIOxDI and interrupt edge detection. Note: The filter circuit consists of a 3-stage DFF and a debounce circuit to filter out positive/negative pulses with a single pulse width less than two filtered sample clocks. (Range of pulse width that can be filtered: 42ns~580ns@Fsys=48MHz)	0x0

3.1.5.13 GPIOx output set register (GPIOxDOSET)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	DOS	Px[7:0] output set control bit write: 0= Unaffected 1= GPIOxDO corresponding bit output high (This register is a write-only register and is invalid for reading)	0x0

3.1.5.14 GPIOx output clear register (GPIOxDOCLR)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	DOC	Px[7:0] output clear control bit write: 0= Unaffected 1= GPIOxDO corresponding bit output low (This register is a write-only register and is invalid for reading)	0x0

3.1.5.15 GPIOx drive current set register (GPIOxDR)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	DR	Px[7:0] drive current set bit 0= Large drive current 1= Small drive current	0Xff

3.1.5.16 GPIOx output rate setting register (GPIOxSR)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	SR	Px[7:0] output rate setting bit 0= The output rate is fast 1= The output rate is slow	0Xff

3.2 Watchdog Timer (WDT)

3.2.1 Overview

The watchdog timer is designed to reset the system when it is running to an unknown state. This practice prevents the system from entering into an indefinite dead-end loop. In addition, the watchdog timer supports the system wake-up function from sleep/deep sleep mode.

3.2.2 Features

- 32-bit free downward counter.
- WDT_CLK=40KHz.
- Support WDT interrupt and WDT reset function.
- With WDT register write protection to avoid abnormal operation.

3.2.3 Feature description

WDT can be set in the user configuration to start after power-on reset of the WDT counter and WDT overflow reset enable (WDTEN=00H after reset), which requires the user configuration bit CONFIG_EN_WDT to be enabled.

After the system reset is completed, WDTLOAD loads the data in the user configuration WDT_TIME, that is, the WDTLOAD default is determined by the WDT_TIME. The WDT overflow time defined by the user can not be defined by the WDT_TIME by modifying the value of the WDTLOAD.

The overflow time is calculated as: $T_{WDTOVER}$=WDTLOAD× count clock period (select the watchdog clock via WDTCON [3:2]).

If the CONFIG_EN_WDT is set to disabled, the power-on reset of the WDT counter defaults to the stop count state, and there are 2 ways to make the WDT counter start counting after the reset is completed:

1) Write a value that is not equal to 5AH to WDTEN (WDT Reset Enable Control Bit).
2) Write 1 to WDTIEN (WDT Interrupt Enable Control Bit).

If the system has a WDT reset, the power-on configuration process is re-performed after the WDT reset, and the reset time is about 4.5ms. After the reset, the WDT count is started and then the WDT reset is started, the time is determined by the WDTLOAD. The interval between the two resets is about 4.5 ms+2×$T_{WDTOVER}$.

After the WDT starts the counter, the 32-bit counter starts at the initial value and counts down. When the count reaches 0, a WDT interrupt is generated, the initial value is automatically loaded, and the downward count is re-counted. When the second interrupt is generated and the last interrupt flag bit is not cleared, a WDT reset is generated (required to be enabled).

3.2.4 Register mapping

(WDT base address = 0x4780_0000) RO: read only; WO: write only; R/W: read and write.

Register	Offset value	R/W	Description	Reset value
CON(P1D)	0x000	R/W	WDT control register	0x00005A00
LOAD(P1D)	0x004	R/W	WDT initial value register	-
VAL	0x008	RO	WDT count value	0Xffffffff
RIS	0x00c	RO	WDT interrupt source status register	0x0
MIS	0x010	RO	WDT enabled interrupt status register	0x0
ICLR(P1D)	0x014	WO	WDT interrupt clear register	-
LOCK	0x500	R/W	WDT write-protect register	0x0

Note: (P1D): The registers marked are protected registers.

- (P1D): When LOCK=55AA6699H, the marked register is allowed to write; = Other values, forbidden to write.

3.2.5 Register description

3.2.5.1 WDT control register (WDTCON)

Bit	Symbol	Description	Reset value
31:17	-	Reserved	-
16	DEBUG	DEBUG mode control 0: WDT stop count when the simulation state is paused 1: The WDT count is independent of the simulation state	0x0
15:8	WDTEN	WDT reset enable 0x5A: Disable WDT reset Other value: Enable WDT reset. When WDT interrupt occurs without clearing the interrupt flag bit, WDT reset will be triggered when WDT interrupt occurs next time. When reset is enabled, WDT interrupt will be enabled regardless of whether WDTCON [0] is 1 or not.	0x5A
7:4	-	Reserved	-
3:2	WDTPRE	WDT clock selection 0x0: WDT_CLK/1 0x1: WDT_CLK/16 0x2: WDT_CLK/256 0x3: Reserved	0x0
1	-	Reserved	-
0	WDTIEN	WDT interrupt enable 0: Disable WDT Interrupt 1: Enable WDT interrupt	0x0

3.2.5.2 WDT initial register (WDTLOAD)

Bit	Symbol	Description	Reset value
31:0	WDTLOAD	WDT count initial value The minimum value is 1	-

3.2.5.3 WDT count value (WDTVAL)

Bit	Symbol	Description	Reset value
31:0	WDTVAL	WDT counter current value	0Xffffffff

3.2.5.4 WDT interrupt source status register (WDTRIS)

Bit	Symbol	Description	Reset value
31:1	-	Reserved	-
0	WDTRIS	1: Generate WDT count down overflow interrupt 0: No interruptions generated	0x0

3.2.5.5 WDT enabled interrupt status register (WDTMIS)

Bit	Symbol	Description	Reset value
31:1	-	Reserved	-
0	WDTMIS	1: Enable WDT interrupt and generate interrupt 0: No interruptions generated	0x0

3.2.5.6 WDT interrupt clear register (WDTICLR)

Bit	Symbol	Description	Reset value
31:0	WDTICLR	Write 0x55AA55AA: Clear the interrupt flag bit and reload the initial value Other value: Unaffected	-

3.2.5.7 WDT write protection register (WDTLOCK)

Bit	Symbol	Description	Reset value
31:0	WDTREN	Write 0x55AA6699: Enable the operation of the WDT-related registers and read as 0x01 Other value: Disable the operation of WDT-related registers and read as 0x00	0x0

3.3 Windowed watchdog timer (WWDT)

3.3.1 Overview

The Windowed Watchdog Timer (WWDT) is used to perform a system reset within a specific window time to prevent the program from running into an uncontrollable state under unpredictable conditions.

3.3.2 Features

- The 6-bit down-count value (CNTDAT) and the 6-bit window comparison value (CMPDAT) make the window period more flexible.
- Supports 4-bit value (PSCSEL) selection window watchdog prescale value, and the prescale counter can reach up to 14 bits.

3.3.3 Feature description

When the WWDT is enabled, the 6-bit counter counts down starting from 0x3F, which triggers a WWDT reset:

1) When performing a reload operation when WWDTVAL > CMPDAT.
2) When the WWDTVAL is reduced to 0x00.

Time to overflow when the WWDT counter counts from 0x3F to 0: (PSCSEL×1024×64) × T_{APBCLK}.

The reload operation can only be performed when CMPDAT>=WWDTVAL>0 will not cause a WWDT reset. When an interrupt is enabled, WWDTVAL=CMPDAT generates an interrupt (it is recommended to perform a reload operation in the interrupt service program before clearing the interrupt flag).

3.3.4 Register mapping

(WWDT base address = 0x4180_0000) RO: read only; WO: write only; R/W: read and write.

Register	Offset value	R/W	Description	Reset value
CON	0x000	R/W	WWDT control registers	0x80000000
RL	0x004	WO	WWDT reload register	-
VAL	0x008	RO	WWDT count value	0x3F
RIS	0x00c	RO	WWDT interrupt source status register	0x0
MIS	0x010	RO	The WWDT enabled interrupt status register	0x0
ICLR	0x014	WO	WWDT interrupt clear register	-

3.3.5 Register description

3.3.5.1 WWDT control register (WWDTCON)

Bit	Symbol	Description	Reset value
31	DEBUG	0: When the simulation state is paused, the WWDT count is not affected 1: When the simulation state is paused, the WWDT count is paused	1
30:22	-	Reserved	-
21:16	CMPDAT	Window comparison value	0x0
15:8	-	Reserved	-
7:4	PSCSEL	0000: Divided by 2 0001: Divided by 4 0010: Divided by 8 0011: Divided by 16 0100: Divided by 32 0101: Divided by 64 0110: Divided by 128 0111: Divided by 256 1000: Divided by 512 1001: Divided by 1024 1010: Divided by 2048 1011: Divided by 4096 1100: Divided by 8192 1101: Divided by 16384 1110: Divided by 16384 1111: Divided by 16384	0x0
3	-	Reserved	-
2	WWDTRF	0: No WWDT reset occurred 1: A WWDT reset occurred	0x0
1	WWDTIEN	WWDT interrupt enable 0: Disable WWDT Interrupt 1: Enable WWDT interrupt	0x0
0	WWDTEN	WWDT enable 0: Disable WWDT module 1: Enable WWDT module	0x0

3.3.5.2 WWDT reload register (WWDTRL)

Bit	Symbol	Description	Reset value
31:0	WWDTRL	Write 0x55AA, reload WWDT count value to 0x3F	-

3.3.5.3 WWDT count value (WWDTVAL)

Bit	Symbol	Description	Reset value
31:6	-	Reserved	-
5:0	WDTVAL	WDT counter current value	0x3F

3.3.5.4 WWDT interrupt source status register (WWDTRIS)

Bit	Symbol	Description	Reset value
31:1	-	Reserved	-
0	WWDTRIS	1: Generate WWDT match interrupt 0: No interruptions generated	0x0

3.3.5.5 WWDT enabled interrupt status register (WWDTMIS)

Bit	Symbol	Description	Reset value
31:1	-	Reserved	-
0	WWDTMIS	1: Enable WWDT interrupt and generate interrupt 0: No interruptions generated	0x0

3.3.5.6 WWDT interrupt clear register (WWDTICLR)

Bit	Symbol	Description	Reset value
31:1	-	Reserved	-
0	WDTICLR	Write 1 to clear the interrupt flag bit Other value: Unaffected	-

3.4 Cyclic Redundancy Check Unit (CRC)

3.4.1 Overview

In order to ensure safety during operation, the IEC61508 standard requires that data be confirmed even during CPU operation. This universal CRC performs CRC operations as a peripheral function. The universal CRC is not limited to the code flash memory area and can be used for multi-purpose inspection. Specify the data to be confirmed by the program.

3.4.2 Features

The CRC-generated polynomial uses CRC-16-CCITT “$X^{16}+X^{12}+X^5+1$”.

3.4.3 Feature description

After writing the CRCIN register, a PCLK clock is needed to save the CRC operation result to the CRCD register. If necessary, you need to read the data of the previous operation before writing, otherwise it will be overwritten by the new operation result.

Example:

Transmit data 12345678H, starting from LSB to MSB.

Transmit order	**0001_1110**	**0110_1010**	**0010_1100**	**0100_1000**	**Transmit by bit from left to right**
	↓	↓	↓	↓	Bitwise in reverse order in bytes
Reverse order result	0111_1000	0101_0110	0011_0100	0001_0010	
CRCIN data	78H ->	56H ->	34H ->	12H	Input to CRCIN data
	↓				Polynomial operation 4 times
CRC result	0000_1000_1111_0110				
	↓				
CRCD data	08F6H				Hexadecimal

Considering the LSB priority communication method, the bit order of the input data is reversed and then calculated. The data “12345678H” is transmitted from the LSB, and the value is written to the CRCIN register in the order of “78H”, “56H”, “34H” and “12H”., and finally the value “08F6H” is read from the CRCD register. This is the result of CRC operation after reversing the bit order of “12345678H”.

3.4.4 Register mapping

(CRC base address =0x4A00_0000)

RO: read only, WO: write only, R/W: read and write

Register	Offset value	R/W	Description	Reset value
CRCIN	0x000	R/W	CRC input register	0x0
CRCD	0x004	R/W	CRC data register	0x0

3.4.5 Register description

3.4.5.1 CRC input register (CRCIN)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	CRCIN	The 8-bit data to be calculated is input by the CRC.	0x0

3.4.5.2 CRC data register (CRCD)

Bit	Symbol	Description	Reset value
31:16	-	Reserved	-
15:0	CRCD	The 16-bit result of the operation is saved by the CRC.	0x0

3.5 Divider (HWDIV)

3.5.1 Overview

The chip contains a 32-bit/32-bit hardware divider.

3.5.2 Features

- Support division of unsigned/signed numbers
- The quotient and remainder are both 32-bit wide
- Clear flag indicator bit
- 6 HCLK clocks for fastest operation completion
- Write division register Initiate division operation

3.5.3 Feature description

The divider can select signed mode or unsigned mode through register HWDIVCON[1], and the divider quotient register HWDIVQ and the remainder register HWDIVR can save the complement of the operation result in signed mode HWDIVCON[1]; It is possible to determine whether the divisor is 0 by register HWDIVCON[2], which is a read-only bit; At the same time, the divider can be determined by register HWDIVCON[3], which is a read-only bit, and a read value of 0 indicates that the divider is operating, 1 indicates that the divider is complete, and the bit is also 1 when the divider is idle.

Note that the clock enable bit of the divider is set in register APBCKEN.

3.5.4 Register mapping

(HWDIV base address = 0x5500_0000)

R RO: read only, WO: write only, R/W: read and write

Register	Offset value	R/W	Description	Reset value
CON	0x000	R/W	Divider control register	0x0
DIVD	0x004	R/W	Divider dividend register	0x0
DIVS	0x008	R/W	Divider divisor register	0x0
DIVQ	0x00C	RO	Divider quotient register	0x0
DIVR	0x010	RO	Divider remainder register	0x0

3.5.5 Register description

3.5.5.1 Divider control register (HWDIVCON)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3	READY	Divider completion indicator bit 0: Divider operation 1: Divider operation is completed or in idle state	0x0
2	DIVBY0	Divider clear indicator bit 0: The divisor is not 0 1: The divisor is 0 (The bit is updated automatically after the division operation is completed)	0x0
1	SIGN	Divider symbol select bit 0: Unsigned mode 1: Signed mode	0x0
0	-	Reserved	-

3.5.5.2 Divider dividend register (HWDIVD)

Bit	Symbol	Description	Reset value
31:0	DIVIDEND	32-bit dividend	0x0

3.5.5.3 Divider divisor register (HWDIVS)

Bit	Symbol	Description	Reset value
31:0	DIVISOR	32-bit divisor	0x0

3.5.5.4 Divider quotient register (HWDIVQ)

Bit	Symbol	Description	Reset value
31:0	QUOTIENT	32-bit quotient	0x0

3.5.5.5 Divider remainder register (HWDIVR)

Bit	Symbol	Description	Reset value
31:0	REMAINDER	32-bit remainder	0x0

3.6 Timers (TIMER0/1)

3.6.1 Overview

Two programmable 32-bit/16-bit counters, namely TIMER0 and TIMER1, provide users with a convenient timing counting function.

3.6.2 Features

- Configurable 32-bit/16-bit down counter.
- Each timer has a separate prescaler.
- Provides three counting operation modes: single trigger, cycle counting, and continuous counting.
- Support chip wake-up from sleep mode.

3.6.3 Feature description

3.6.3.1 Single trigger mode

If the timer is operating in single trigger mode, after enabling the timer, the counter loads the initial value from the loading register, counts down, and when the counter is decremented to 0, it stops working and produces an interrupt. To start the single trigger mode again, you need to zero out the TMROS bit and then set the TMROS bit.

(When starting the single trigger mode again, it should be noted that when the TMROS bit is cleared, the time to remain 0 must be greater than a timer count period)

3.6.3.2 Cycle count mode

If the timer works in cycle count mode, after enabling the timer, the counter loads the initial value from the loading register and counts down, and when the counter decreases to 0, the counter loads the initial value from the loading register and continues counting, while producing an interrupt.

3.6.3.3 Continuous count mode

If the timer works in continuous count mode, after enabling the timer, the counter loads the initial value from the loading register, counting down, and when the counter is decremented to 0, the counter loads the maximum value as the initial value and continues counting while generating an interrupt.

3.6.3.4 Lazy loading function

When data is written to the load register, the counter does not continue to decrement, it loads the initial value from the load register on the rising edge of the next TIMER_CLK, and then decrements the count.

When data is written to the lazy load register, the data is written to the load register on the rising edge of the next TIMER_CLK, and if the counter has begun to count, it waits for the current cycle count to be 0 before loading the initial value from the load register.

3.6.4 Register mapping

(Timer0 base address= 0x4680_0000; Timer1 base address= 0x4680_0100)

O: read only; WO: write only; R/W: read and write

Register	Offset value	R/W	Description	Reset value
CON	0x000	R/W	Timer control register	0x20
LOAD	0x004	R/W	Timer loading register	0x0
VAL	0x008	RO	Timer current value register	0Xffffffff
RIS	0x00c	RO	Timer interrupt source status register	0x0
MIS	0x010	RO	Timer enabled interrupt status register	0x0
ICLR	0x014	WO	Timer interrupt clear register	-
BGLOAD	0x018	R/W	Timer delay loading register	0x0

3.6.5 Register description

3.6.5.1 Timer control register (TIMERxCON)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7	TMREN	Timer enable bit 0: Disable 1: Enable	0x0
6	TMRMS	Timer mode select bit 0: Continuous count mode 1: Cycle count mode	0x0
5	TMRIE	Timer interrupt enable bit 0: Disable interrupt 1: Enable interrupt	1
4	-	Reserved	-
3:2	TMRPRE	Timer prescaler 00: Divided by 1 01: Divided by 16 10: Divided by 256 11: Reserved	0x0
1	TMRSZ	Timer count bit selection 0: 16-bit counter 1: 32-bit counter	0x0
0	TMROS	Single trigger mode select bit 0: The mode is determined by the TRMS bit 1: Single-shot trigger mode (Single-shot mode is triggered again, the initial value of which is determined by the TRMS bit)	0x0

3.6.5.2 Timer loading register (TIMERxLOAD)

Bit	Symbol	Description	Reset value
31:0	TMRxLOAD	Timer loading register	0x0

3.6.5.3 Timer current value register (TIMERxVAL)

Bit	Symbol	Description	Reset value
31:0	TMRxVAL	Timer current count value	0Xffffffff

3.6.5.4 Timer interrupt source status register (TIMERxRIS)

Bit	Symbol	Description	Reset value
31:1	-	Reserved	-
0	TMRxRIS	Timer interrupt source status 1: Generate an interrupt 0: No interruptions generated	0x0

3.6.5.5 Timer enabled interrupt status register (TIMERxMIS)

Bit	Symbol	Description	Reset value
31:1	-	Reserved	-
0	TMRxMIS	Timer enabled Interrupt status bit 1: Interrupt enables and produces interrupts 0: No interruptions generated	0x0

3.6.5.6 Timer interrupt clear register (TIMERxICLR)

Bit	Symbol	Description	Reset value
31:0	TMRxICLR	Write any number, clear the timer interrupt	-

3.6.5.7 Timer delay loading register (TIMERxBGLOAD)

Bit	Symbol	Description	Reset value
31:0	TMRxBGLOAD	Timer lazy load register (the read value is the value of the last time TMRxLOAD or TIMERxBGLOAD is written).	0x0

3.7 Capture/compare/PWM module (CCP0/1)

3.7.1 Overview

It contains 2 groups of CCP modules CCP0/CCP1, and each group of CCP corresponds to channel A and channel B. CCP0 corresponds to CCP0A/CCP0B, and CCP1 corresponds to CCP1A/CCP1B.

3.7.2 Features

- Up to 2 CCPs with up to 4 PWM outputs.
- Each CCP can be set with an independent period.
- The CCPn has an internal 16-bit counter that generates a compare/overflow interrupt.
- The CCPn has an independent capture function, with the option of inputting the signal on either the A or B pin.
- The CCP1 has a 4-channel capture function, which can capture CCP0A/CCP0B/CCP1A/CCP1B input signals simultaneously.
- Capture mode 1 supports the reload CCP0 counter function for capture operations.
- The internal channel CAP3 supports analog comparator output capture.
- Internal channel CAP0-CAP3 supports software capture function.

3.7.3 Feature description

3.7.3.1 Pulse width modulation mode (PWM)

Each set of CCP can output A and B two PWMs: PWMxA, PWMxB, these two channels share a cycle, the output duty cycle can be set independently through CCPDxA, CCPDxB. PWMxA/PWMxB output polarity can be set by PWMxAO/PWMxBOP bits, corresponding to CCPxA/CCPxB channel output.

When the CCPx run bit is set to 1, the 16-bit counter loads the value of the CCPx Reload Register and counts down. When the count value equals to the value of CCPDxA/B, the PWMxA/PWMxB output level is changed.

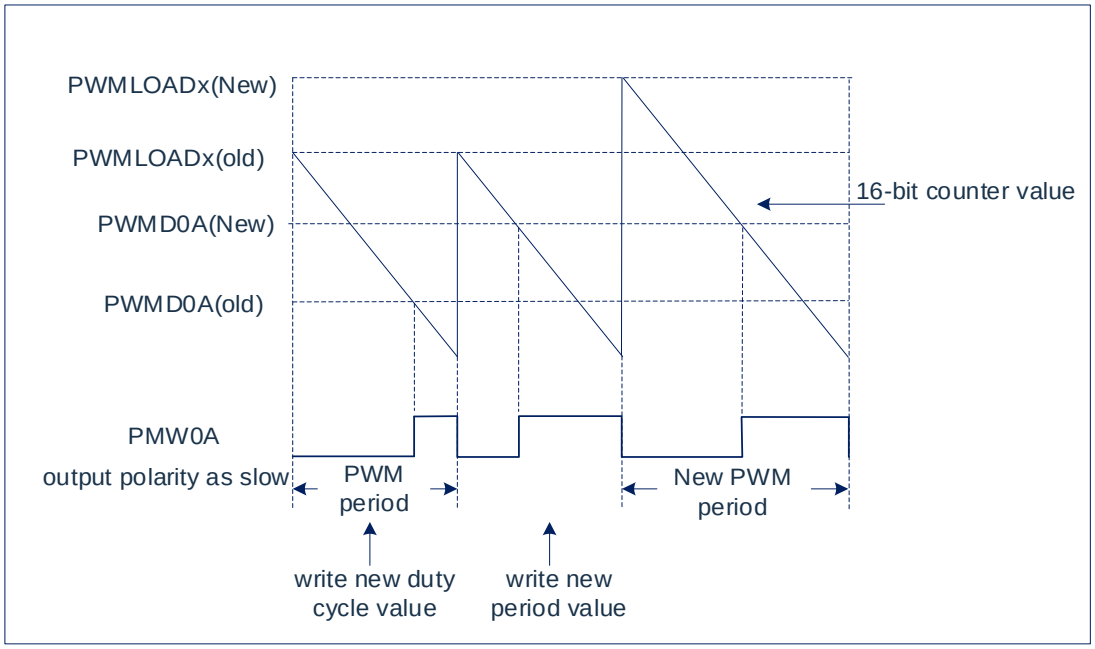


Figure 3-1: PWM timing diagram

Periods and duty cycles are calculated as follows:

Period = CCPLOAD× CCP clock period

PWMxA duty cycle = CCPDxA/CCPLOADx (supports 0%~100%)

PWMxB duty cycle = CCPDxB/CCPLOADx (supports 0%~100%)

When CCP LOADx=0, PWMxA, PWMxB duty cycle is 0%.

WHEN CCPDxA> CCPLOADx is, the duty cycle is 100%.

3.7.3.2 Capture mode 0

The capture mode is external capture.

Each set of CCP can be set from A or B as an external capture signal pin, after the CCPRUNx is set, the 16-bit count starts from the 0xFFFF and counts down, when the capture condition is triggered, the counter stops counting, and the CCPxA or CCPxB returns the value of the current counter. If you need to perform the next capture, you need to clear the CCP RUNx and then set it.

The capture time is calculated as follows:

CCPLOADx.RELOAD=0, capture time=(0xFFFF -CCPDxA/B) ×CCPx clock period

CCPLOADx.RELOAD=1, capture time=(CCPxLOAD[15:0]-CCPDxA/B) × CCPx clock period

3.7.3.3 Capture mode 1

The CCP1 includes 4 internal channels such as CAP0, CAP1, CAP2, CAP3. One of the channels can be selected as the capture channel either in the external channel ECAP00-03 or ECAP10-13. You can also select CCP0A/CCP0B/CCP1A/CCP1B as the capture channel.

The ECAP00-03 corresponds to the positive input C0P0-C0P3 of analog comparator0.

The ECAP10-13 corresponds to the positive input C1P0-C1P3 of analog comparator1.

When using ECAP external capture, the corresponding port needs to be set to GPIO function.

When using CCP0A/CCP0B/CCP1A/CCP1B capture, the corresponding port needs to be set as a CCP port.

Correspondence between CAPn and external channels:

Internal channel	External channel	
CAP0	CAP0CHS=n:	Select ECAP0n (n=0-3)@ECAPS=0
	CAP0CHS=n:	Select ECAP1n (n=0-3)@ECAPS=1
	CAP0CHS=F:	Select CAP0A
	CAP0CHS=Other value:	Reserved
CAP1	CAP1CHS=n:	Select ECAP0n (n=0-3)@ECAPS=0
	CAP1CHS=n:	Select ECAP1n (n=0-3)@ECAPS=1
	CAP1CHS=F:	Select CAP0B
	CAP1CHS=Other value:	Reserved
CAP2	CAP2CHS=n:	Select ECAP0n (n=0-3)@ECAPS=0
	CAP2CHS=n:	Select ECAP1n (n=0-3)@ECAPS=1
	CAP2CHS=F:	Select CAP1A
	CAP2CHS=Other value:	Reserved
CAP3	CAP3CHS=n:	Select ECAP0n (n=0-3)@ECAPS=0
	CAP3CHS=n:	Select ECAP1n (n=0-3)@ECAPS=1
	CAP3CHS=8:	Select the ACMP0 filter to select the output after selection
	CAP3CHS=9:	Select the ACMP1 filter to select the output after selection
	CAP3CHS=F:	Select CAP1B
	CAP3CHS=Other value:	Reserved

In capture mode 1, PWM mode outputs for CCP0 and CCP1 and external capture mode 0 are disabled.

This mode requires CCP1 to operate in count mode, and the capture operation loads the CCP1 count median into the associated registers.

In addition, CCP0 can optionally operate in count mode, and the CAP0-CAP3 capture trigger loading function can be set separately. That is, when the channel is set up to have a capture operation generated, the counter initial value of CCP0 will be reloaded. Multiple channels can set the function at the same time, and software-triggered capture does not reload the initial value of CCP0.

In capture mode 1, the compare/overflow interrupt function of CCP0 and CCP1 can be used normally.

There are two types of capture methods: an external signal trigger capture and a software trigger capture.

1) External signal trigger capture:

Both CAP0-CAP3 can be selected for rising/falling edge or double edge capture. When a signal is generated, the value of the CCP1 counter is captured into the corresponding register and an interrupt flag is generated. The correspondence of the 4 channels to the capture register is as follows:

CAP0/CAP1/CAP2/CAP3 correspond to cap0DAT/CAP1DAT/CAP2DAT/CAP3DAT registers, respectively.

2) Software triggered capture:

Write operations to CAP0DAT-CAP3DAT generate capture operations on the CAP0-CAP3 channels. Capture the value of the CCP1 counter to the corresponding register. And the 31-16 bits written must be 0x55AA to trigger the capture operation. The low 16-bit data written is not correlated. Software-triggered capture does not produce an interrupt flag.

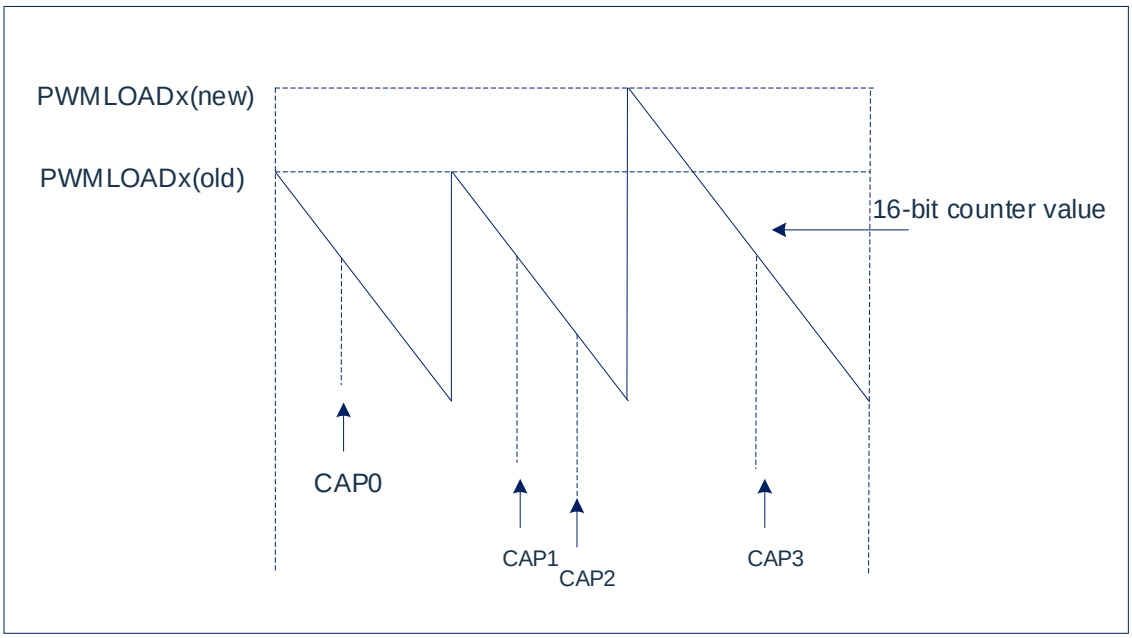


Figure 3-2: CAP0-CAP3 channel capture operation

3.7.3.4 PWM configuration process

- Configure the PWM control registers, set the prescale, select the PWM mode, and enable PWM.
- Configure the PWM cycle to write to the CCPLOADx registers.
- Configure the PWM duty cycle to write to the CCPDxA/CCPDxB registers.
- If an interrupt is required, enable the associated interrupt bits and clear the interrupt status register.
- Set the corresponding I/O port to the PWM output.
- Set the PWM run register to start the output.

3.7.3.5 Interrupt

In PWM mode, CCPx can generate two types of interrupts:

- When the counter is decremented to 0, an underflow interrupt is generated.
- A comparison interrupt occurs when the value of the counter is equal to the value of CCPDxA or CCPDxB.

At capture mode 0/1, two types of interrupts can be generated:

- When the counter is decremented to 0, an underflow interrupt is generated.
  When a capture condition is triggered, a capture interrupt is generated.

3.7.4 Register mapping

(CCP base address = 0x4280_0000) RO: read only; WO: write only; R/W: read and write.

Register	Offset value	R/W	Description	Reset value
CCPCON0(P1B)	0x000	R/W	CCP0 control register	0x0
CCPLOAD0(P1A)	0x004	R/W	CCP0 reload register	0x0
CCPD0A(P1A)	0x008	R/W	CCP0 channel A data register	0x0
CCPD0B(P1A)	0x00c	R/W	CCP0 channel B data register	0x0
CCPCON1(P1B)	0x010	R/W	CCP1 control register	0x0
CCPLOAD1(P1A)	0x014	R/W	CCP1 reload register	0x0
CCPD1A(P1A)	0x018	R/W	CCP1 channel A data register	0x0
CCPD1B(P1A)	0x01C	R/W	CCP1 channel B data register	0x0
-	0x030	-	Reserved	-
-	0x034	-	Reserved	-
-	0x038	-	Reserved	-
-	0x03C	-	Reserved	-
CCPIMSC(P1B)	0x040	R/W	CCP interrupt enable register	0x0
CCPRIS	0x044	RO	CCP interrupt source status register	0x0
CCPMIS	0x048	RO	THE CCP enabled interrupt status register	0x0
CCPICLR	0x04C	WO	CCP interrupt clear register	0x0
CCPRUN(P1B)	0x050	R/W	CCP run register	0x0
CCPLOCK	0x054	R/W	CPP0/1 write enable register	0x0
CAPCON(P1B)	0x058	R/W	Capture control register	0x0
CAPCHS(P1B)	0x05C	R/W	Capture channel selection register	0x0
CAP0DAT0(P1A)	0x060	R/W	Capture channel 0 data register	0x0
CAP1DAT0(P1A)	0x064	R/W	Capture channel 1 data register	0x0
CAP2DAT0(P1A)	0x068	R/W	Capture channel 2 data register	0x0
CAP3DAT0(P1A)	0x06C	R/W	Capture channel 3 data register	0x0

Note:
(P1A/P1B) The registers marked are protected registers.
- (P1A): When LOCK=55H or AAH, the marked register allows writing; = Other values, forbidden to write.
- (P1B): When LOCK=55H, the labeled register is allowed to write; = Other values, forbidden to write.

3.7.5 Register description

3.7.5.1 CCPx control register (CCPCONx)x=0,1

Bit	Symbol	Description	Reset value
31:7	-	Reserved	-
6	CCPxEN	CCPx enable bit 0: Disable 1: Enable	0x0
5:4	CCPxPS	CCPx prescale selection 0x0: PCLK 0x1: PCLK/4 0x2: PCLK/16 0x3: PCLK/64	0x0
3	CCPxMS	CCPx mode selection 0: Capture mode 0 (effective when CAPEN=0). 1: PWM mode (effective when CAPEN=0).	0x0
2	CCPxCM0CS	CCPx capture mode 0 capture channel selection 0: Channel CCPxA 1: Channel CCPxB	0x0
1:0	CCPxCM0ES	CCPx capture mode 0 capture mode selection 0x0: CCPRUNx=1 starts counting, rises along the capture and produces an interrupt 0x1: CCPRUNx=1 starts counting, drops along the capture and produces an interrupt 0x2: The rising edge starts counting, and the falling edge captures and produces an interrupt 0x3: The falling edge starts counting, and the rising edge captures and produces an interrupt	0x0

3.7.5.2 CCP reload register (CCPLOADx)x=0,1

Bit	Symbol	Description	Reset value
31:17	-	Reserved	-
16	RELOAD	CCP0 module: PWM mode: Reload enable bit 0: The counter reload value is 0xFFFF 1: The counter reload value is CCP0LOAD Capture mode 0: 0: The counter reload value is 0xFFFF 1: The counter reload value is CCP0LOAD CCP1 module: PWM mode: Reload enable bit 0: The counter reload value is 0xFFFF 1: The counter reload value is CCP1LOAD Capture mode 0,1: 0: The counter reload value is 0xFFFF 1: The counter reload value is CCP1LOAD	0x0
15:0	CCPxLOAD	Load value for CCPx counter (recommended load value is not 0)	0x0

3.7.5.3 CCPxA data register (CCPDxA)x=0,1

Bit	Symbol	Description	Reset value
31:17	-	Reserved	-
16	PWMxAOP	PWMxA output polarity selection 0: Normal output 1: Reverse output	0x0

15:0	CCPxADATA	PWM mode: Duty cycle of PWMxA Capture mode 0: Capture result	0x0

3.7.5.4 CCPxB data register (CCPDxB)x=0,1

Bit	Symbol	Description	Reset value
31:17	-	Reserved	-
16	PWMxBOP	PWMxB output polarity selection 0: Normal output 1: Reverse output	0x0
15:0	CCPxBDATA	PWM mode: Duty cycle of PWMxB Capture mode 0: Capture result	0x0

3.7.5.5 CCP Iinterrupt enable register (CCPIMSC)

Bit	Symbol	Description	Reset value
31:12	-	Reserved	-
11	CAP3IMSC	CAP3 capture interrupt enable bit 0: Disable 1: Enable	0x0
10	CAP2IMSC	CAP2 capture interrupt enable bit 0: Disable 1: Enable	0x0
9	CAP1IMSC	CAP1 capture interrupt enable bit 0: Disable 1: Enable	0x0
8	CAP0IMSC	CAP0 capture interrupt enable bit 0: Disable 1: Enable	0x0
7:6	-	Reserved	0x0
5	PWMIMSC	PWM1 overflow interrupt enable bit 0: Disable 1: Enable	0x0
4	PWMIMSC4	PWM0 overflow interrupt enable bit 0: Disable 1: Enable	0x0
3:2	-	Reserved	-
1	PWMIMSC1	PWM1 compare/capture interrupt enable bit 0: Disable 1: Enable	0x0
0	PWMIMSC0	PWM0 compare/capture interrupt enable bit 0: Disable 1: Enable	0x0

3.7.5.6 CCP interrupt source status register (CCPRIS)

Bit	Symbol	Description	Reset value
31:12	-	Reserved	-
11	CAP3RIS	CAP3 capture interrupt status bit 1: An interrupt is generated 0: No interruptions generated	0x0
10	CAP2RIS	CAP2 capture interrupt status bit 1: An interrupt is generated 0: No interruptions generated	0x0
9	CAP1RIS	CAP1 capture interrupt status bit 1: An interrupt is generated 0: No interruptions generated	0x0
8	CAP0RIS	CAP0 capture interrupt status bit 1: An interrupt is generated 0: No interruptions generated	0x0
7:6	-	Reserved	0x0
5	PWMRIS5	PWM1 overflow interrupt status bit 1: An interrupt is generated 0: No interruptions generated	0x0
4	PWMRIS4	PWM0 overflow interrupt status bit 1: An interrupt is generated 0: No interruptions generated	0x0
3:2	-	Reserved	-
1	PWMRIS1	PWM1 compare/capture interrupt status bit 1: An interrupt is generated 0: No interruptions generated	0x0
0	PWMRIS0	PWM0 compare/capture interrupt status bit 1: An interrupt is generated 0: No interruptions generated	0x0

3.7.5.7 CCP enabled interrupt status register (CCPMIS)

Bit	Symbol	Description	Reset value
31:12	-	Reserved	-
11	CAP3MIS	CAP3 enabled capture interrupt status bit 1: Interrupt enable and generate Interrupts 0: No interruptions generated	0x0
10	CAP2MIS	CAP2 enabled capture interrupt status bit 1: Interrupt enable and generate Interrupts 0: No interruptions generated	0x0
9	CAP1MIS	CAP1 enabled capture interrupt status bit 1: Interrupt enable and generate Interrupts 0: No interruptions generated	0x0
8	CAP0MIS	CAP0 enabled capture interrupt status bit 1: Interrupt enable and generate Interrupts 0: No interruptions generated	0x0
7:6	-	Reserved	-
5	PWMMIS5	PWM1 enabled overflow interrupt status bit 1: Interrupt enable and generate Interrupts 0: No interruptions generated	0x0
4	PWMMIS4	PWM0 enabled overflow interrupt status bit 1: Interrupt enable and generate Interrupts 0: No interruptions generated	0x0
3:2	-	Reserved	-
1	PWMMIS1	PWM1 enabled compare/capture interrupt status bit 1: Interrupt enable and generate Interrupts 0: No interruptions generated	0x0
0	PWMMIS0	PWM0 enabled compare/capture interrupt status bit 1: Interrupt enable and generate Interrupts 0: No interruptions generated	0x0

3.7.5.8 CCP interrupt clear register (CCPICLR)

Bit	Symbol	Description	Reset value
31:12	-	Reserved	-
11	CAP3ICLR	Write 1 to clear the CAP3 capture interrupt status bit	0x0
10	CAP2ICLR	Write 1 to clear the CAP2 capture interrupt status bit	0x0
9	CAP1ICLR	Write 1 to clear the CAP1 capture interrupt status bit	0x0
8	CAP0ICLR	Write 1 to clear the CAP0 capture interrupt status bit	0x0
7:6	-	Reserved	-
5	PWMICLR5	Write 1 to clear the PWM1 overflow interrupt status bit	0x0
4	PWMICLR4	Write 1 to clear the PWM0 overflow interrupt status bit	0x0
3:2	-	Reserved	-
1	PWMICLR1	Write 1 to clear the PWM1 compare/capture interrupt status bit	0x0
0	PWMICLR0	Write 1 to clear the PWM0 compare/capture interrupt status bit	0x0

3.7.5.9 CCP run register (CCPRUN)

Bit	Symbol	Description	Reset value
31:2	-	Reserved	-
1	CCPRUN1	CCP1 run control bit 0: Stop 1: Run	0x0
0	CCPRUN0	CCP0 run control bit 0: Stop 1: Run	0x0

3.7.5.10 CCP write enable control register (CCPLOCK)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	LOCK	When LOCK=0x55, enable the registers with protection level P1B. When LOCK=0Xaa, enable the operation of registers with protection level P1B and P1A. When LOCK=other value, operation of registers with protection level is prohibited.	0x0

3.7.5.11 CAP control register (CAPCON)

Bit	Symbol	Description	Reset value
31:13	-	Reserved	-
12	CAPEN	Capture mode 1 enable bit 0: CCP0/CCP1 enabled for PWM mode or capture mode 0 1: Capture mode 1 enabled, i.e. full channel capture mode CCP0 switches to programmable continuous count mode. CCP1 switches to programmable continuous count mode	0x0
11	CAP3RLEN	CAP3 capture in capture mode 1 triggers the CCP0 counter load enable bit 0: Disable 1: Enabled, (requires capture mode 1 and is in effect in CCP0 operating state). When a capture trigger signal occurs in CAP3, CCP0 will reload the data in the CCP0LOAD register during the operation of the counter.	0x0
10	CAP2RLEN	CAP2 capture in capture mode 1 triggers the CCP0 counter load enable bit 0: Disable 1: Enabled, (requires capture mode 1 and is in effect in CCP0 operating state) When a capture trigger signal occurs in CAP2, CCP0 will reload the data in the CCP0LOAD register during the operation of the counter.	0x0
9	CAP1RLEN	CAP1 capture in capture mode 1 triggers the CCP0 counter load enable bit 0: Disable 1: Enabled, (requires capture mode 1 and is in effect in CCP0 operating state) When a capture trigger signal occurs in CAP1, CCP0 will reload the data in the CCP0LOAD register during the operation of the counter.	0x0
8	CAP0RLEN	CAP0 capture in capture mode 1 triggers the CCP0 counter load enable bit 0: Disable 1: Enabled, (requires capture mode 1 and is in effect in CCP0 operating state) When a capture trigger signal occurs in CAP0, CCP0 will reload the data in the CCP0LOAD register during the operation of the counter.	0x0
7:6	CAP3ES	CAP3 capture mode selection 0x0: Disable 0x1: Rising edge capture 0x2: Falling edge capture 0x3: Both rising edge and falling edge	0x0
5:4	CAP2ES	CAP2 capture mode selection 0x0: Disable 0x1: Rising edge capture 0x2: Falling edge capture 0x3: Both rising edge and falling edge	0x0
3:2	CAP1ES	CAP1 capture mode selection 0x0: Disable 0x1: Rising edge capture 0x2: Falling edge capture 0x3: Both rising edge and falling edge	0x0
1:0	CAP0ES	CAP0 capture mode selection 0x0: Disable 0x1: Rising edge capture 0x2: Falling edge capture	0x0

		0x3: Both rising edge and falling edge	

3.7.5.12 CAP channel selection register (CAPCHS)

Bit	Symbol	Description	Reset value
31:17	-	Reserved	-
16	ECAPS	ECAP capture channel group selection 0: Select ECAP00-ECAP03 1: Select ECAP10-ECAP13	0x0
15:12	CAP3CHS	CAP3 capture channel selection 0x0: ECAPx0 (x = 0 or 1, determined by ECAPS) 0x1: ECAPx1 0x2: ECAPx2 0x3: ECAPx3 0x4: Disable 0x5: Disable 0x8: The output of ACMP0 (non-event output). 0x9: The output of ACMP1 (non-event output). 0Xf: CCP1B Other value: Reserved	0x0
11:8	CAP2CHS	CAP2 capture channel selection 0x0: ECAPx0 (x = 0 or 1, determined by ECAPS) 0x1: ECAPx1 0x2: ECAPx2 0x3: ECAPx3 0x4: Disable 0x5: Disable 0Xf: CCP1A Other value: Reserved	0x0
7:4	CAP1CHS	CAP1 capture channel selection 0x0: ECAPx0 (x = 0 or 1, determined by ECAPS) 0x1: ECAPx1 0x2: ECAPx2 0x3: ECAPx3 0x4: Disable 0x5: Disable 0Xf: CCP0B Other value: Reserved	0x0
3:0	CAP0CHS	CAP0 capture channel selection 0x0: ECAPx0 (x = 0 or 1, determined by ECAPS) 0x1: ECAPx1 0x2: ECAPx2 0x3: ECAPx3 0x4: Disable 0x5: Disable 0Xf: CCP0A Other value: Reserved	0x0

3.7.5.13 CAP data register (CAPnDAT0) (n=0-3)

Bit	Symbol	Description	Reset value
31:16	-	Read: Invalid Write: 0x55AA, generated a capture operation for CAPn Write: Other values are invalid	0x0
15:0	CAPnDATA	Read: Capture the 16bit value of the CCP1 counter for CAPn Write: Invalid	0x0

3.8 Enhanced PWM (EPWM)

3.8.1 Overview

The enhanced PWM module supports six PWM generators, which can be configured as six independent PWM outputs (EPWM0-EPWM5) or as three pairs of complementary PWM (EPWM0-EPWM1, EPWM2-EPWM3, EPWM4-EPWM5) with programmable dead-zone generators.

Each pair of PWMs shares an 8-bit prescaler with 6 clock dividers that provide 5 divider factors (1, 1/2, 1/4, 1/8, 1/16). Each PWM output is controlled by a separate 16-bit counter, and a 16-bit comparator is used to adjust the duty cycle. The 6-channel PWM generator provides 24 interrupt flags, and the period or duty cycle of the relevant PWM channel matches the counter and will produce interrupt flags, with each PWM having a separate enable bit.

Each PWM can be configured as a single mode (which generates a PWM signal cycle) or a cyclic mode (continuous output of the PWM waveform).

3.8.2 Features

The Enhanced PWM Module has the following features:

- 6 independent 16-bit PWM control modes.
  - 6 independent outputs: EPWM0, EPWM1, EPWM2, EPWM3, EPWM4, EPWM5;
  - 3 sets of complementary PWM pairs: (EPWM0-EPWM1), (EPWM2-EPWM3), (EPWM4-EPWM5), programmable dead-zone can be inserted;
  - 3 sets of synchronous PWM pairs: (EPWM0-EPWM1), (EPWM2-EPWM3), (EPWM4-EPWM5), each set of PWM pairs pin synchronization.
- Support group control, EPWM0, EPWM2, EPWM4 output synchronization, EPWM1, EPWM3, EPWM5 output synchronization.
- Single mode (edge alignment only) or auto-load mode.
- Support edge aligned mode and center aligned mode.
- Center aligned mode supports symmetric count and asymmetric count.
- Programmable dead-zone generators are supported in complementary PWMs.
- Each PWM has independent polarity control.

3.8.3 Feature description

Description:

- Period point: When the counter CNTn is counted to equal to the period PERIODn, it is called the period point. The resulting interrupt is PIFn.
- Zero point: When the counter CNTn counts to 0, it is called the zero point. The resulting interrupt is ZIFn.
- Up-compare point: When the counter CNTn is counted to equal to CMPDATn, it is called the up-compare point. The resulting interrupt is UIFn. Edge alignment counts have no up-compare points.
- Down-compare point: When the counter CNTn is subtracted to equal to CMPDATn or CMPDDATn, it is called a down-compare point. The resulting interrupt is DIFn.
- Midpoint: The midpoint is the middle point, and when the midpoint is centered on the counting method, the CNTn counts to a moment equal to the CMPDATn or CMPDDATn, and because the CNTn will be subtracted to 0, the moment is called the midpoint, which is also the period point. Edge alignment count has no midpoint, but has a period point.

Note:

1) When the edges are aligned, the period data is loaded at the beginning of the first count, which will produce a period point; At other moments, after the counter counts to 0, the period data needs to be loaded immediately. So, the subsequent period point is the same as the position of the zero point. There is a down comparison point for this alignment, not an up comparison point.
2) When the center is aligned, the first count starts counting upwards from 0 and results in a zero point. When the period data is counted, a period point (midpoint) is generated. The zero point alternates with the midpoint. The alignment has an upward comparison point and a downward comparison point, and when the symmetry is counted, the upward comparison point and the downward comparison point are determined by CMPDATn; For asymmetric counting, the upward comparison point is determined by CMPDATn and the downward comparison point is determined by CMDDATn.

3.8.3.1 Block diagram

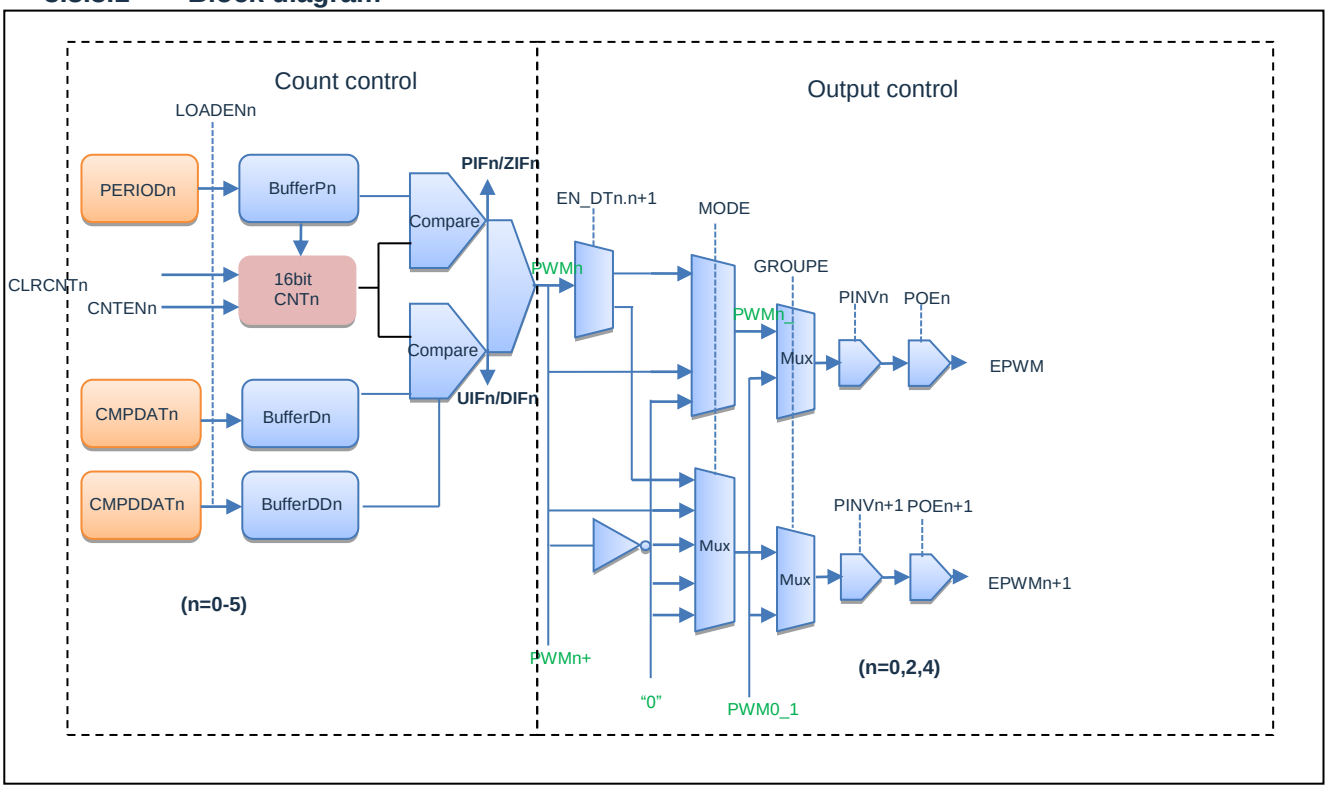


Figure 3-3: EPWM block diagram

3.8.3.2 Clock divider

Each pair of PWMs shares an 8-bit prescaler, and after the prescale, each PWM can choose (1, 1/2, 1/4, 1/8, 1/16) 5 divider ratios.

PWM_CLK = PCLK / (CLKPSCxx + 1) / CLKDIVn, where xx can be 01, 23, 45, n=0-5.

3.8.3.3 Independent output mode

The six EPWM channel outputs do not affect each other and operate according to their respective cycle/duty cycle data.

3.8.3.4 Complementary output mode

In the complementary output mode, the six PWMs are divided into 3 pairs, EPWM0 is 1 pair with EPWM1, EPWM2 is 1 pair with EPWM3, and EPWM4 is 1 pair with EPWM5. There are 3 pairs of PWM in total.

EPWM0-EPWM1 operates on EPWM0 period/duty cycle data, and EPWM0 is inverted from the EPWM1 waveform.

EPWM2-EPWM3 operates on EPWM2 period/duty cycle data, and EPWM2 is inverted from the EPWM3 waveform.

EPWM4-EPWM5 operates on EPWM4 period/duty cycle data, and EPWM4 is inverted from the EPWM5 waveform.

In this mode, the EPWM1/EPWM3/EPWM5 outputs are independent of their own associated operating data registers, but the output control is still valid. Such as output enable, mask, brake and other controls.

Dead-zone delay control is supported in complementary mode.

3.8.3.5 Synchronous output mode

In synchronous output mode, the six PWMs are divided into 3 pairs, EPWM0 is paired with EPWM1, EPWM2 is paired with EPWM3, and EPWM4 is paired with EPWM5. There are 3 pairs of PWM in total.

EPWM0-EPWM1 operates on the period/duty cycle data of EPWM0, which is in phase with EPWM1 waveform.

EPWM2-EPWM3 operates on the period/duty cycle data of EPWM2, which is in phase with EPWM3 waveform.

EPWM4-EPWM5 operates on the period/duty cycle data of EPWM4, which is in phase with EPWM5 waveform.

In this mode, the EPWM1/EPWM3/EPWM5 outputs are independent of their own associated operating data registers, but the output control is still valid. Such as output enable, mask, brake and other controls.

3.8.3.6 Group output mode

GROUPEN=1 enables the group function, 6 channels of PWM are divided into 2 groups, EPWM0, EPWM2, EPWM4 is 1 group, EPWM1, EPWM3, EPWM5 is another group.

EPWM0-EPWM2-EPWM4 operates on EPWM0 period/duty cycle data, with 3 channels in phase.

EPWM1-EPWM3-EPWM5 operates on EPWM0 period/duty cycle data, with 3 channels in phase.

When the grouping function is turned on, the EPWM2/EPWM3/EPWM4/EPWM5 outputs are independent of their own associated run data registers, but the output control is still effective. For example, output enable control.

3.8.3.7 Load update mode

There are two counter loading modes: one-shot mode and continuous mode (auto loading mode)

Single mode:

The cycle duty cycle related data is loaded once at the beginning of the counter, and the output PWM period is related to the loading method.

- When LOADTYPn=0, the edge alignment is 1 period and the center alignment is 0.5 periods.
- When LOADTYPn=1, the edge alignment is 2 periods and the center alignment is 1 period.
- When LOADTYPn=2, the edge alignment is 3 periods and the center alignment is 1.5 periods.
- When LOADTYPn=3, the edge alignment is 4 periods and the center alignment is 2 periods.

Continuous mode:

The period, duty cycle data is automatically loaded at the zero and midpoints of the PWM period. Midpoint loading exists only in center alignment count mode.

In edge alignment counting mode, a zero point is generated at the same time as a period point, and the count comparison circuit reloads the value of CMPDATn/PERIODn/CMPTGD0/CMPTGD1.

In center-align count mode, both the midpoint and the zero point are automatically loaded with values for the associated registers. Such a structure supports the first half waveform cycle duty cycle and the second half waveform cycle duty cycle.

Due to the dual cache structure of EPWM, during EPWM operation, the value of the relevant operating registers: CMPDATn/CMPDDATn/PERIODn/CMPTGD0/CMPTGD1 is changed, the PWM output waveform does not change immediately, and the values of these registers are loaded into the corresponding cache only at the zero or period point.

Such a structure does not immediately change the output waveform in the current PWM cycle or half-cycle after changing the period duty cycle data, and the PWM waveform will not change accordingly in the next cycle or half-cycle. That is, any changes in PWM-related data do not affect the current full PWM cycle or half-cycle.

In high-speed applications, it is possible that the load point has arrived, but the operation of writing to the operating register has not yet been completed. At this point, you do not expect some of the running data to have been loaded and another part of the running data to be unloaded.

For this high-speed application. The EPWM module provides a loading enable bit, after changing the relevant operating register, you need to set the load enable bit LOADENn to 1, and the LOADENn bit is automatically cleared after loading. This bit can also be read to determine whether the value of the associated register is loaded into the actual circuit. If LOADENn= 0, it means that it has been loaded, which will affect the PWM waveform being output; If LOADENn=1, it means that the current PWM waveform has not yet changed, and the value of the register that changed before the next load point will be loaded. If you change the value of the associated run register again, you also need to reset LOADENn to 1.

By default, PWM loads the operating data of the relevant registers at both the zero and period points, and generates zero and periodic interrupts. In order to adapt to more flexible application requirements. PWM supports different loading modes and zero/period point interrupt generation.

In register EPWMCON3 LOADTYPn(0-5) can be set the load mode and the interrupt mode at the zero/period point:

LOADTYEn	Center alignment loading	Edge alignment loading
00	Each zero and period point is loaded with and produces zero and periodic interrupt flags	Each zero or period point is loaded with zero and periodic interrupt flags
01	Each zero point is loaded with a zero interrupt flag	Every 2 zeros are loaded with a zero interrupt flag
10	The first zero point is loaded alternately with the next cycle point, resulting in a zero and period point interrupt flag	Every 3 zeros or period points are loaded with a zero and periodic interrupt flag
11	Every two zeros are loaded with a relevant zero interrupt flag	Every 4 zeros are loaded with a zero interrupt flag

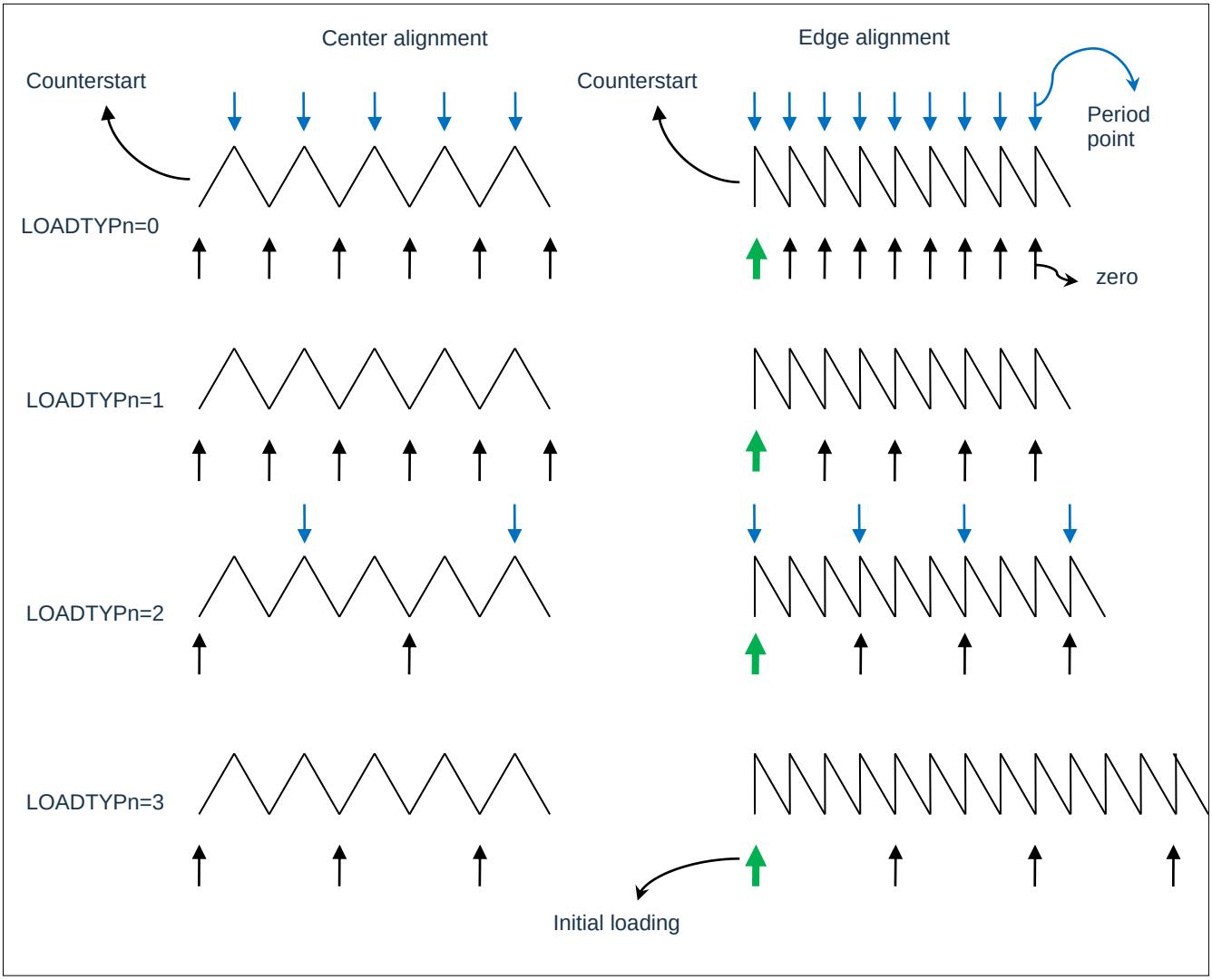


Figure 3-4: PWM period/duty cycle loading update block diagram

3.8.3.8 Edge alignment count mode

In edge alignment mode, the counting method is down, that is, minus 1 count. The 16-bit PWM counter CNTn counts down at the beginning of each cycle, compared to the latched CMPDATn value, and when CNTn= CMPDATn, the EPWMn output is high, cmPnDIF is set to 1. CNTn continues to count down to 0, at which point EPWMn will output low, the current CMPDATn and PERIODn will be reloaded at PWMnCNTM=1, and the PIF cycle interrupt flag will be set.

The relevant parameters for edge alignment are as follows:

$$\text{High voltage duration} = (\text{CMPDATn}+1) \times \text{Tpwm}$$

$$\text{Period} = (\text{PERIODn}+1) \times \text{Tpwm}$$

$$\text{Duty cycle} = \frac{\text{CMPDATn}+1}{\text{PERIODn}+1}$$

If CMPDATn > PERIODn, the duty cycle is 100%, and the EPWMn channel is always high. And there is no down-to-compare interrupt.

If CMPDATn= 0, the duty cycle is 0%.

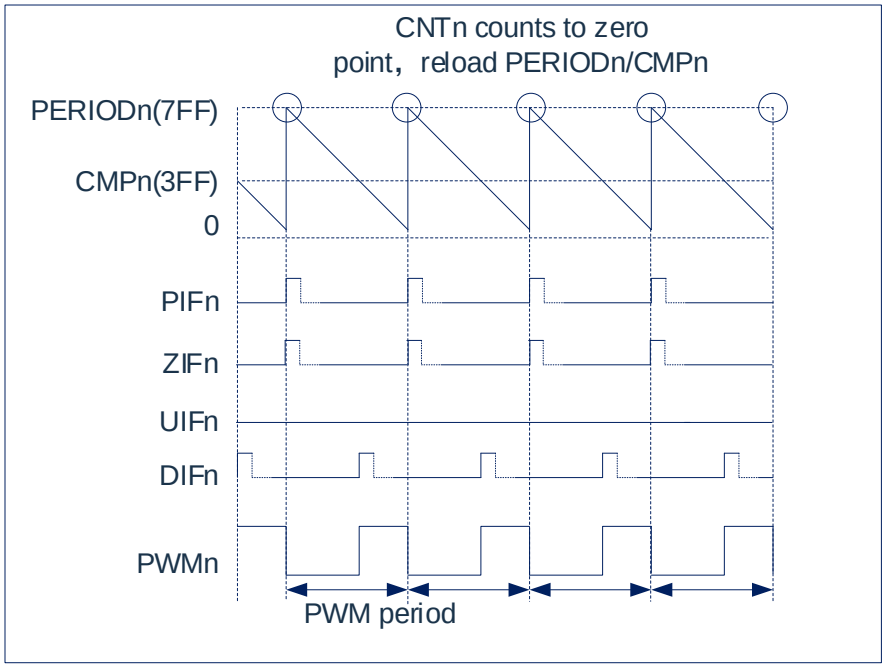


Figure 3-5: Edge alignment mode waveform plot

3.8.3.9 Center alignment count mode

In center-align mode, the counting method is counting up and then counting down.

The center alignment mode is divided into two symmetrical ways: symmetrical counting mode and asymmetric counting mode.

The symmetric count mode (ASYMEN=0) duty cycle is determined by CMPDATAn.

The asymmetric count mode (ASYMEN=1) duty cycle is determined by CMPDATAn and CMPDDATn.

Under the center-aligned symmetrical counting mode, the 16-bit PWM counter CNTn starts from 0 to count upwards, when CNTn = CMPDATn, EPWMn outputs a high level, after which CNTn continues to count upwards to equal to PERIODn, and then CNTn begins to count down, in the process of counting down CNTn= CMPDATn, EPWMn outputs a low level, and then continues to count down to 0.

$$High\ voltage\ duration = (PERIODn \times 2 - CMPDATn \times 2 - 1) \times Tpwm$$

$$Period = (PERIODn) \times 2 \times Tpwm$$

$$Duty\ cycle = \frac{PERIODn \times 2 - CMPDATn \times 2 - 1}{PERIODn \times 2}$$

If CMPDATn > = PERIODn, the duty cycle is 0%, the EPWMn channel is always low, and there is no upward comparison interrupt or downward comparison interrupt.

If PERIODn=0, the duty cycle is 0%, the EPWMn channel is always low, and the zero-point interrupt and the period point interrupt are always present when CNTn is enabled.

If CMPDATn=0, the duty cycle is 100%.

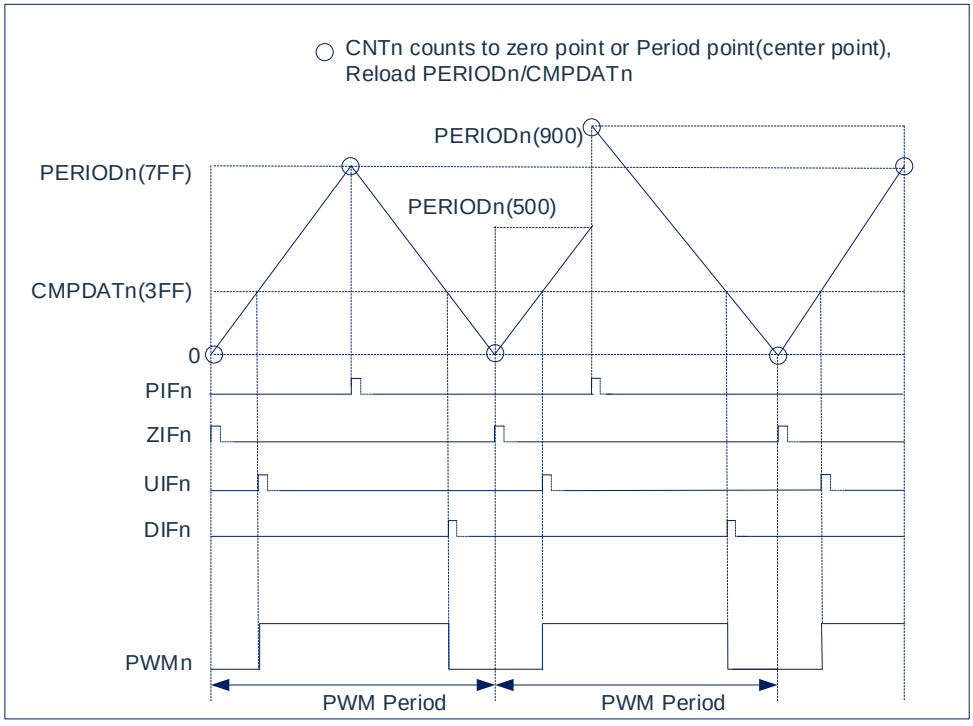


Figure 3-6: Center alignment mode symmetrical counting waveform plot

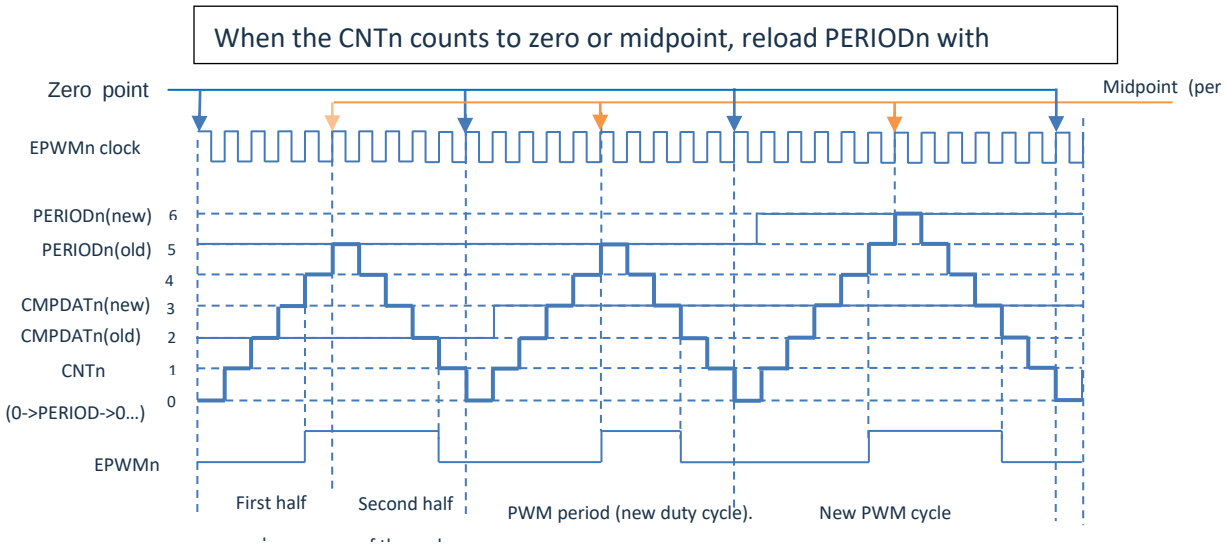


Figure 3-7: Center-aligned counter waveform (symmetrical count).

In the center-aligned asymmetric counting mode, the 16-bit PWM counter CNTn starts counting up from 0, when CNTn= CMPDATn, EPWMn outputs a high level, after which CNTn continues to count up to equal to PERIODn, and then CNTn begins to count down, in the process of counting down CNTn= CMPDDATn, EPWMn outputs a low level, and then continues to count down to 0. To enable the asymmetric counting method, the ASYMEN needs to be set to 1, and the asymmetric counting method can achieve accurate center alignment waveforms.

The relevant parameters for the center-aligned asymmetric count are as follows:

High voltage duration = $(PERIODn\times2-CMPDDATn-CMPDATn-1)\times Tpwm$

Period = $(PERIODn)\times2\times Tpwm$

Duty cycle = $\frac{PERIODn\times2-CMPDDATn-CMPDATn-1}{PERIODn\times2}$, $(CMPDATAn<PERIODn, CMPDDATn<PERIODn)$

Duty cycle = $\frac{PERIODn-CMPDDATn-1}{PERIODn\times2}$, $(CMPDATAn\geq PERIODn, CMPDDATn<PERIODn)$

Duty cycle = $\frac{PERIODn-CMPDATn}{PERIODn\times2}$, $(CMPDATAn<PERIODn, CMPDDATn\geq PERIODn)$

Duty cycle=0%, $(CMPDATAn\geq PERIODn, CMPDDATn\geq PERIODn)$

CMPDATAn > =PERIODn does not produce an upward comparison interrupt.

CMPDDATAn does not produce a downward comparison interrupt when > =PERIODn.

If PERIODn=0, the duty cycle is 0%, the EPWMn channel is always low, and the zero-point interrupt and the period point interrupt are always present when CNTn is enabled.

If CMPDATn=0 and CMDATDn=0, the duty cycle is 100%.

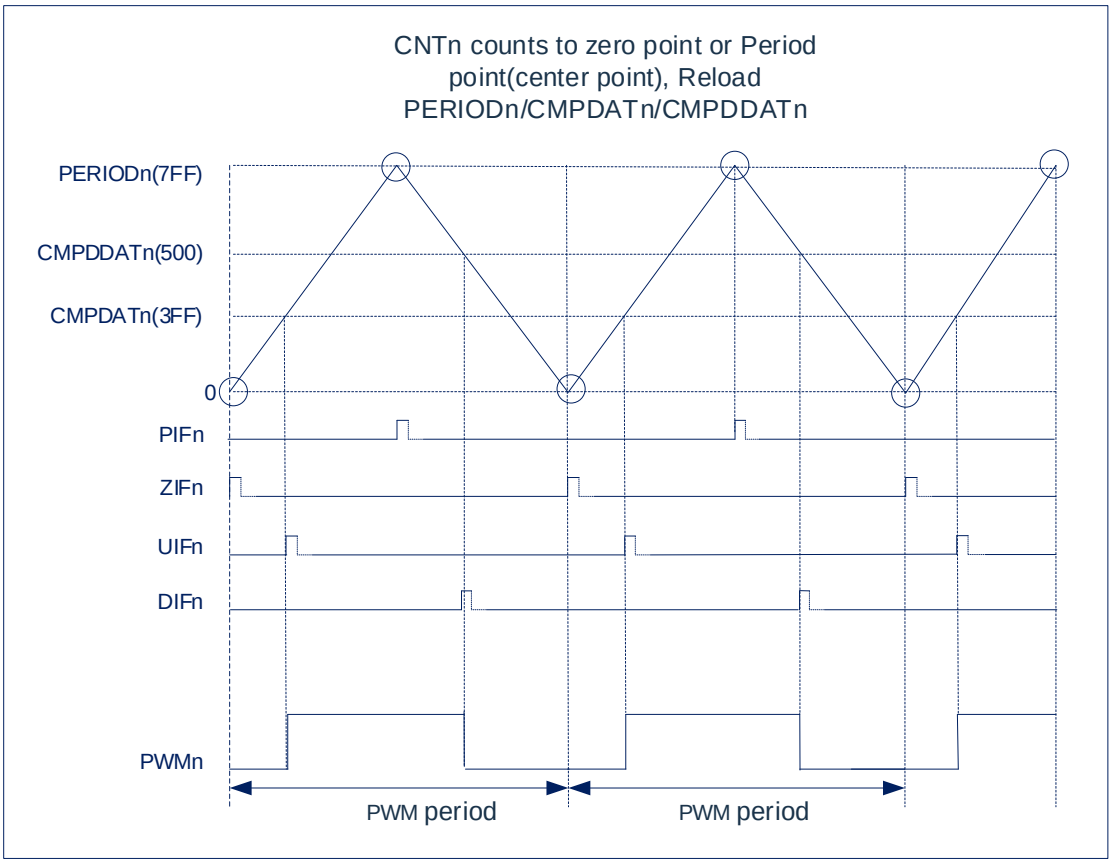


Figure 3-8: Asymmetric count waveform plot in center alignment mode

3.8.3.10 Programmable dead-zone generator

The 6-channel PWM can be set to 3 sets of complementary pairs. In the complementary output mode, the period and duty cycle of PWM1, PWM3, and PWM5 are determined by the PWM0, PWM2, and PWM4 relevant registers, respectively, and the dead-zone delay registers can also affect the duty cycle of the PWM complementary pair. In addition to the corresponding output enable control bit (PWMnOE), the PWM1/PWM3/PWM5 output waveform is no longer controlled by its own registers.

In complementary mode, each set of complementary PWM pairs supports inserting a dead-zone delay, and the inserted dead-zone time is as follows:

PWM0/1 Dead-zone: (PWM01DT [9:0] +1) $\times T_{PWM0}$

PWM2/3 Dead-zone: (PWM23DT [9:0]+1) $\times T_{PWM2}$

PWM4/5 Dead-zone: (PWM45DT [9:0]+1) $\times T_{PWM4}$

$T_{PWM0}/T_{PWM2}/T_{PWM4}$ are the clock source periods of PWM0/PWM2/PWM4, respectively.

Dead-zone time can be set from 0.021us to 21us (Fpwmn=48MHz)

The output mode does not affect the counter's mode, so both center alignment and edge alignment support complementary output modes.

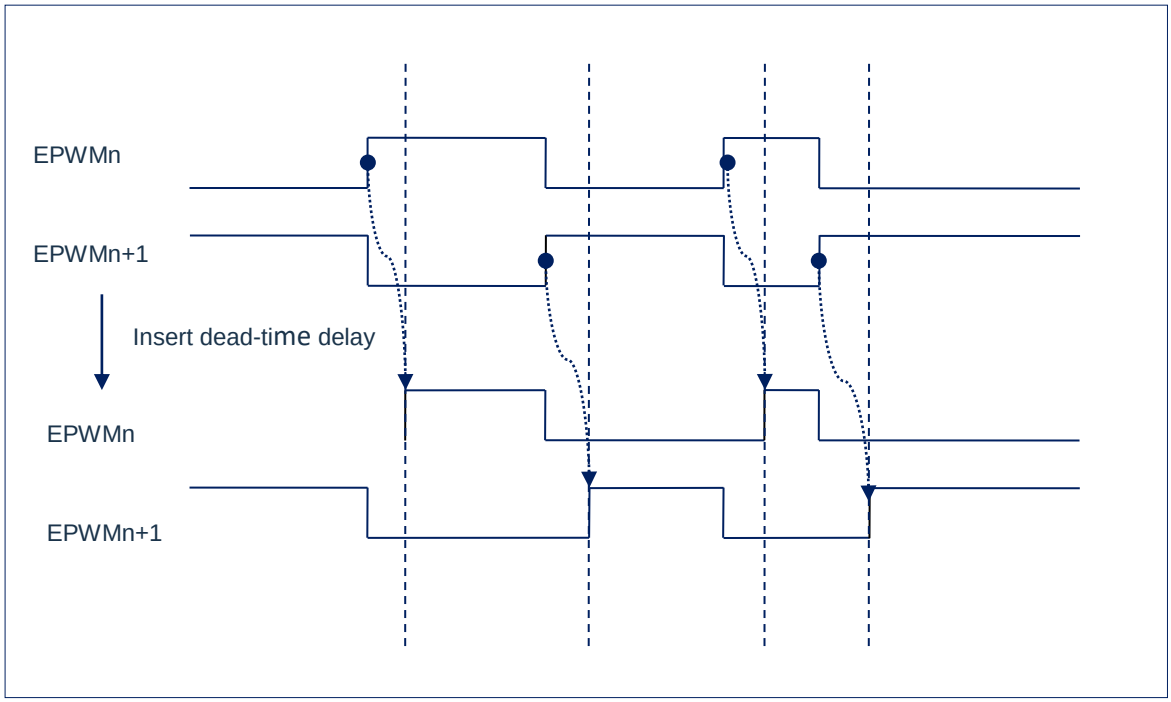


Figure 3-9: Both center alignment and edge alignment support complementary output modes

3.8.3.11 EPWM configuration process

1) Write 0x55 lock registers to enable EPWM register operations
2) Configure the EPWM clock divider to set the prescale ratio and independent frequency division ratio
3) Select Mode, Independent Mode, or Complementary Mode
4) Set the EPWM period and duty cycle
5) Set the EPWM output polarity
6) Enable the EPWM counter
7) Configure the relevant IO port as the EPWM function port
8) Enable the associated EPWM channel output
9) Write 0x00 to the LOCK register to avoid misoperation of the EPWM-related registers until the next time the EPWM-related registers need to be operated and then re-enable them.

3.8.3.12 Interrupt

The EPWM unit has four interrupt sources:

- ZIFn—Interrupt flag generated when the EPWM counter counts to zero
- UIFn—The EPWM counter counts up to the CMPDATn interrupt flag
- PIFn—The EPWM counter edges align the count interrupt flags and the center aligns the count interrupt flags
- DIFn—The EPWM counter counts down to the CMPDATn/CMPDDATn interrupt flag

All interrupt flags are hardware-set and must be cleared by software.

3.8.4 Register mapping

(EPWM base address =0x4A80_0000) RO: read only, WO: write only, R/W: read and write

Register	Offset value	R/W	Description	Reset value
CLKPSC(P1B)	0x000	R/W	EPWM prescaler register	0x0
CLKDIV(P1B)	0x004	R/W	EPWM clock selection register	0x0
CON(P1B)	0x008	R/W	EPWM control register	0x0
CON2(P1B)	0x00C	R/W	EPWM control register 2	0x0
CON3(P1B)	0x010	R/W	EPWM control register 3	0x0
PERIOD0(P1A)	0x014	R/W	EPWM cycle register 0	0x0
PERIOD1(P1A)	0x018	R/W	EPWM cycle register 1	0x0
PERIOD2(P1A)	0x01C	R/W	EPWM cycle register 2	0x0
PERIOD3(P1A)	0x020	R/W	EPWM cycle register 3	0x0
PERIOD4(P1A)	0x024	R/W	EPWM cycle register 4	0x0
PERIOD5(P1A)	0x028	R/W	EPWM cycle register 5	0x0
CMPDAT0(P1A)	0x02C	R/W	EPWM comparison register 0	0x0
CMPDAT1(P1A)	0x030	R/W	EPWM comparison register 1	0x0
CMPDAT2(P1A)	0x034	R/W	EPWM comparison register 2	0x0
CMPDAT3(P1A)	0x038	R/W	EPWM comparison register 3	0x0
CMPDAT4(P1A)	0x03C	R/W	EPWM comparison register 4	0x0
CMPDAT5(P1A)	0x040	R/W	EPWM comparison register 5	0x0
POEN(P1B)	0x048	R/W	EPWM output control register	0x0
-	0x04C	-	Reserved	-
DTCTL(P1B)	0x050	R/W	EPWM dead-zone length register	0x0
IMSC(P1B)	0x064	R/W	EPWM interrupt enable register	0x0
RIS	0x068	RO	EPWM interrupt source status register	0x0
MIS	0x06c	RO	EpWM enabled Interrupt status register	0x0
ICLR	0x070	WO	EPWM interrupt clear register	0x0
IFA(P1B)	0x074	R/W	EPWM interrupt accumulate control register	0x0
LOCK	0x078	R/W	EPWM write enable control register	0x0

Note: (P1A/P1B) The registers marked are protected registers.

- (P1A): When LOCK=55H or AAH, the marked register allows writing; = Other values, forbidden to write.
- (P1B): When LOCK=55H, the labeled register is allowed to write; = Other values, forbidden to write.

3.8.5 Register description

3.8.5.1 EPWM prescaler register (CLKPSC)

Bit	Symbol	Description	Reset value
31:24	-	Reserved	-
23:16	CLKPSC45	EPWM counter 4 and 5 clock prescaler CLK_PSC45 = PCLK/(CLKPSC45+1) f the CLKPSC45=0, the prescaler has no clock output, and the CLKDIVn bit does not work if the clock associated with the PSC is selected	0x0
15:8	CLKPSC23	EPWM counters 2 and 3 clock prescalers CLK_PSC23 = PCLK/(CLKPSC23+1) If the CLKPSC23=0 and the prescaler have no clock output, the COUNTER does not work if the CLKDIVn bit selects a clock associated with the PSC	0x0
7:0	CLKPSC01	EPWM counter 0 and 1 clock prescaler CLK_PSC01 = PCLK/(CLKPSC01+1) If the CLKPSC01=0, the prescaler has no clock output, and the CLKDIVn bit does not work if the PSC-related clock is selected	0x0

3.8.5.2 EPWM clock selection register (CLKDIV)

Bit	Symbol	Description	Reset value
31:23	-	Reserved	-
22:20	CLKDIV5	Counter 5 clock divider selection 000: CLK_PSC45/2 001: CLK_PSC45/4 010: CLK_PSC45/8 011: CLK_PSC45/16 100: CLK_PSC45/1 Other value: PCLK	0x0
19	-	Reserved	-
18:16	CLKDIV4	Counter 4 clock divider selection 000: CLK_PSC45/2 001: CLK_PSC45/4 010: CLK_PSC45/8 011: CLK_PSC45/16 100: CLK_PSC45/1 Other value: PCLK	0x0
15	-	Reserved	-
14:12	CLKDIV3	Counter 3 clock divider selection 000: CLK_PSC23/2 001: CLK_PSC23/4 010: CLK_PSC23/8 011: CLK_PSC23/16 100: CLK_PSC23/1 Other value: PCLK	0x0
11	-	Reserved	-
10:8	CLKDIV2	Counter 2 clock divider selection 000: CLK_PSC23/2 001: CLK_PSC23/4 010: CLK_PSC23/8	0x0

		011: CLK_PSC23/16 100: CLK_PSC23/1 Other value: PCLK	
7	-	Reserved	-
6:4	CLKDIV1	Counter 1 clock divider selection 000: CLK_PSC01/2 001: CLK_PSC01/4 010: CLK_PSC01/8 011: CLK_PSC01/16 100: CLK_PSC01/1 Other PCLK	0x0
3	-	Reserved	-
2:0	CLKDIV0	Counter 0 clock divider selection 000: CLK_PSC01/2 001: CLK_PSC01/4 010: CLK_PSC01/8 011: CLK_PSC01/16 100: CLK_PSC01/1 Other value: PCLK	0x0

3.8.5.3 EPWM control register (CON)

Bit	Symbol	Description	Reset value
31:26	-	Reserved	-
25:24	MODE	EPWM operation mode selection 00: Independent mode 01: Complementary model 10: Synchronous mode 11: Reserved	0x0
23	GROUNPEN	EPWM group function enable bit 0: All PWM channels are independent of each other 1: EPWM0 controls EPWM2, EPWM4. EPWM1 controls EPWM3,EPWM5	0x0
22	ASYMEN	Asymmetric count enable in EPWM center alignment mode 0: Symmetry count enable 1: Asymmetric count enable	0x0
21	CNTTYPE	EPWM count alignment selection 0: Edge alignment 1: Center alignment	0x0
20	HALT	Counter control bit during HALT (debug) 0: Counter counts normally during HALT 1: Counter stops during HALT	0x0
19	-	Reserved	-
18	EN_DT45	EPWM counter 4 and 5 dead zone enable bit 0: Disable counter 4 and 5 dead zone 1: Enable counter 4 and 5 dead zone	0x0
17	EN_DT23	EPWM counter 2 and 3 dead zone enable bit 0: Disable counter 2 and 3 dead zone	

		1: Enable counter 2 and 3 dead zone	
16	EN_DT01	EPWM counter 0 and 1 dead zone enable bit 0: Disable counter 0 and 1 dead zones 1: Enable counter 0 and 1 dead zones	0x0
15:14	-	Reserved	-
13	PINV5	EPWM5 output polarity control bit 0: Normal output 1: Reverse output	0x0
12	PINV4	EPWM4 output polarity control bit 0: Normal output 1: Reverse output	0x0
11	PINV3	EPWM3 output polarity control bit 0: Normal output 1: Reverse output	0x0
10	PINV2	EPWM2 output polarity control bit 0: Normal output 1: Reverse output	0x0
9	PINV1	EPWM1 output polarity control bit 0: Normal output 1: Reverse output	0x0
8	PINV0	EPWM0 output polarity control bit 0: Normal output 1: Reverse output	0x0
7:6	-	Reserved	-
5	CNTMODE5	EPWM5 autoload/single-shot mode 0: Single-shot mode 1: Auto load mode	0x0
4	CNTMODE4	EPWM4 autoload/single-shot mode 0: Single-shot mode 1: Auto load mode	0x0
3	CNTMODE3	EPWM3 autoload/single-shot mode 0: Single-shot mode 1: Auto load mode	0x0
2	CNTMODE2	EPWM2 autoload/single-shot mode 0: Single-shot mode 1: Auto load mode	0x0
1	CNTMODE1	EPWM1 autoload/single-shot mode 0: Single-shot mode 1: Auto load mode	0x0
0	CNTMODE0	EPWM0 autoload/single-shot mode 0: Single-shot mode 1: Auto load mode	0x0

3.8.5.4 EPWM control register (CON2)

Bit	Symbol	Description	Reset value
31:6	-	Reserved	-
5	CNTEN5	EPWM5 counter enable bit 0: Disable 1: Enable (The bit is cleared automatically after single-shot mode is completed).	0x0
4	CNTEN4	EPWM4 counter enable bit 0: Disable 1: Enable (The bit is cleared automatically after single-shot mode is completed).	0x0
3	CNTEN3	EPWM3 counter enable bit 0: Disable 1: Enable (The bit is cleared automatically after single-shot mode is completed).	0x0
2	CNTEN2	EPWM2 counter enable bit 0: Disable 1: Enable (The bit is cleared automatically after single-shot mode is completed).	0x0
1	CNTEN1	EPWM1 counter enable bit 0: Disable 1: Enable (The bit is cleared automatically after single-shot mode is completed).	0x0
0	CNTEN0	EPWM0 counter enable bit 0: Disable 1: Enable (The bit is cleared automatically after single-shot mode is completed).	0x0

3.8.5.5 EPWM control register (CON3)

Bit	Symbol	Description	Reset value
31:28	-	Reserved	-
27:26	LOADTYP5	EPWM5 load/interrupt mode selection bit 00: Each zero and period point loads and produces an interrupt flag 01: Each zero point is loaded with an interrupt flag 10: The first zero point alternates with the next cycle point to load and produce an interrupt flag Every two zero points are loaded with an interrupt flag 11: Each zero and period point loads and produces an interrupt flag	0x0
25:24	LOADTYP4	EPWM4 load/interrupt mode selection bit 00: Each zero and period point loads and produces an interrupt flag 01: Each zero point is loaded with an interrupt flag 10: The first zero point alternates with the next cycle point to load and produce an interrupt	0x0

		flag 11: Every two zero points are loaded with an interrupt flag	
23:22	LOADTYP3	EPWM3 load/interrupt mode selection bit 00: Each zero and period point loads and produces an interrupt flag 01: The first zero point alternates with the next cycle point to load and produce an interrupt flag 10: Each zero point is loaded with an interrupt flag 11: Every two zero points are loaded with an interrupt flag	0x0
21:20	LOADTYP2	EPWM2 load/interrupt mode selection bit 00: Each zero and period point loads and produces an interrupt flag 01: Each zero point is loaded with an interrupt flag 10: The first zero point alternates with the next cycle point to load and produce an interrupt flag 11: Every two zero points are loaded with an interrupt flag	0x0
19:18	LOADTYP1	EPWM1 load/interrupt mode selection bit 00: Each zero and period point loads and produces an interrupt flag 01: Each zero point is loaded with an interrupt flag 10: The first zero point alternates with the next cycle point to load and produce an interrupt flag 11: Every two zero points are loaded with an interrupt flag	0x0
17:16	LOADTYP0	EPWM0 load/interrupt mode selection bit 00: Each zero and period point loads and produces an interrupt flag 01: Each zero point is loaded with an interrupt flag 10: The first zero point alternates with the next cycle point to load and produce an interrupt flag 11: Every two zero points are loaded with an interrupt flag	0x0
15:14	-	Reserved	-
13	LOADEN5	EPWM5 cycle/comparator load enable bit 0: Disable 1: Enable (automatically cleared to zero by hardware after loading)	0x0
12	LOADEN4	EPWM4 cycle/comparator load enable bit 0: Disable 1: Enable (automatically cleared to zero by hardware after loading)	0x0
11	LOADEN3	EPWM3 cycle/comparator load enable bit 0: Disable 1: Enable (automatically cleared to zero by hardware after loading)	0x0
10	LOADEN2	EPWM2 cycle/comparator load enable bit 0: Disable 1: Enable (automatically cleared to zero by hardware after loading)	0x0

9	LOADEN1	EPWM1 cycle/comparator load enable bit 0: Disable 1: Enable (automatically cleared to zero by hardware after loading)	0x0
8	LOADEN0	EPWM0 cycle/comparator load enable bit 0: Disable 1: Enable (automatically cleared to zero by hardware after loading)	0x0
7:6	-	Reserved	-
5	CNTCLR5	EPWM5 counter clear bit 0: Disable 1: Enable (automatically cleared to zero by hardware)	0x0
4	CNTCLR4	EPWM4 counter clear bit 0: Disable 1: Enable (automatically cleared to zero by hardware)	0x0
3	CNTCLR3	EPWM3 counter clear bit 0: Disable 1: Enable (automatically cleared to zero by hardware)	0x0
2	CNTCLR2	EPWM2 counter clear bit 0: Disable 1: Enable (automatically cleared to zero by hardware)	0x0
1	CNTCLR1	EPWM1 counter clear bit 0: Disable 1: Enable (automatically cleared to zero by hardware)	0x0
0	CNTCLR0	EPWM0 counter clear bit 0: Disable 1: Enable (automatically cleared to zero by hardware)	0x0

3.8.5.6 EPWM period register 0-5(PERIOD0-5)

Bit	Symbol	Description	Reset value
31:16	-	Reserved	-
15:0	PERIODn	EPWMn counter period value	0x0

3.8.5.7 EPWM comparision register 0-5(CMPDAT0-5)

Bit	Symbol	Description	Reset value
31:16	CMPDDATn	EPWMn counter down compare value	0x0
15:0	CMPDATn	EPWMn counter compare value	0x0

3.8.5.8 EPWM output control register (POEN)

Bit	Symbol	Description	Reset value
31:6	-	Reserved	-
5:0	POENn	EPWMn output enable bit 0: EPWM channel n output is disabled 1: EPWM channel n output is enabled	0x0

3.8.5.9 EPWM dead zone length register (DTCTL)

Bit	Symbol	Description	Reset value
31:30	-	Reserved	-
29:20	DTI45	Channel 4 and Channel 5 dead-zone length register Dead zone time= PWM_CLK45×DTI45	0x0
19:10	DTI23	Channel 2 and Channel 3 dead-zone length register Dead zone time = PWM_CLK23×DTI23	0x0
9:0	DTI01	Channel 0 and channel 1 dead-zone length register Dead zone time = PWM_CLK01× DTI01	0x0

3.8.5.10 EPWM interrupt enable register (IMSC)

Bit	Symbol	Description	Reset value
31:30	-	Reserved	-
29:24 n=5-0	EN_DIFn	EPWMn downward compare interrupt enable bit 0: Disable 1: Enable	0x0
23:22	-	Reserved	-
21:16 n=5-0	EN_UIFn	EPWMn upward compare interrupt enable bit 0: Disable 1: Enable	0x0
15:14	-	Reserved	-
13:8 n=5-0	EN_PIFn	EPWMn period interrupt enable bit 0: Disable 1: Enable	0x0
7:6	-	Reserved	-
5:0 n=5-0	EN_ZIFn	EPWMn zero interrupt enable bit 0: Disable 1: Enable	0x0

3.8.5.11 EPWM interrupt source status register (RIS)

Bit	Symbol	Description	Reset value
31:30	-	Reserved	-
29:24 n=5-0	RIS_DIFn	EPWMn downward compare interrupt source status bit 0: No interruptions generated 1: An interrupt is generated	0x0
23:22	-	Reserved	-
21:16 n=5-0	RIS_UIFn	EPWMn upward compare interrupt source status bit 0: No interruptions generated 1: An interrupt is generated	0
15:14	-	Reserved	-
13:8 n=5-0	RIS_PIFn	EPWMn period interrupt source status bit 0: No interruptions generated 1: An interrupt is generated	0x0
7:6	-	Reserved	-
5:0 n=5-0	RIS_ZIFn	EPWMn zero-point interrupt source status bit 0: No interruptions generated 1: An interrupt is generated	0

3.8.5.12 EPWM enabled interrupt status register (MIS)

Bit	Symbol	Description	Reset value
31:30	-	Reserved	-
29:24 n=0-5	MIS_DIFn	EPWMn downward compare enabled interrupt status bit 0: No interruptions generated 1: Enabled and produced an interrupt	0x0
23:22	-	Reserved	-
21:16 n=0-5	MIS_UIFn	EPWMn upward compare enabled interrupt status bit 0: No interruptions generated 1: Enabled and produced an interrupt	0x0
15:14	-	Reserved	-
13:8 n=0-5	MIS_PIFn	EPWMn period enabled interrupt status bit 0: No interruptions generated 1: Enabled and produced an interrupt	0
7:6	-	Reserved	-
5:0 n=0-5	MIS_ZIFn	EPWMn zero-point enabled interrupt status bit 0: No interruptions generated 1: Enabled and produced an interrupt	0x0

3.8.5.13 EPWM interrupt clear control register (ICLR)

Bit	Symbol	Description	Reset value
31:30	-	Reserved	-
29:24 n=0-5	ICLR_DIFn	EPWMn downward compare interrupt clear bit 0: Unaffected 1: Clear the RIS_DIFn flag bit	0x0
23:22	-	Reserved	-
21:16 n=0-5	ICLR_UIFn	EPWMn upward compare interrupt clear bit 0: Unaffected 1: Clear the RIS_UIFn flag bit	0x0
15:14	-	Reserved	-
13:8 n=0-5	ICLR_PIFn	EPWMn period interrupt clear control bit 0: Unaffected 1: Clear the RIS_PIFn flag bit	0x0
7:6	-	Reserved	-
5:0 n=0-5	ICLR_ZIFn	EPWMn zero-point interrupt clear control bit 0: Unaffected 1: Clear the RIS_ZIFn flag bit	0x0

3.8.5.14 EPWM interrupt accumulation control register (IFA)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:4	ZIFCMP	Zero interrupt accumulation comparison value When ZIFn interrupt accumulates to (IFCMP+1), the corresponding interrupt flag of ZIFn is set to 1.	0x0
3:1	-	Reserved	-
0	ZIFAEN	Zero-point interrupt accumulate enable bit 0: Disable 1: Enable	0x0

3.8.5.15 EPWM write enable control register (LOCK)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	LOCK	When LOCK=0x55, enable the operation of other EPWM registers. When LOCK=0Xaa, only the EPWM cycle registers and comparison registers are enabled. When LOCK=other values, operation of EPWM related registers is disabled.	0x0

3.9 Universal asynchronous transceiver (UART0/1)

3.9.1 Overview

It includes 2 universal asynchronous serial interfaces, supports hardware flow control, software flow control, and supports 16-byte transmit and receive FIFO.

3.9.2 Features

- Full-duplex, asynchronous communication.
- Independent 16 bytes to transmit/receive FIFO.
- Support hardware automatic flow control (CTS, RTS).
- Support software flow control function (XOFF, XON).
- Receive buffer trigger level can be selected.
- Programmable serial interface features.
  - The data bit length can be set to 5 to 8 bits.
  - The check digits can be set to be parity, no check, or fixed check bits for generation and detection.
  - The stop bit length can be set to 1 bit, 1.5 bits, or 2 bits.

3.9.3 Feature description

3.9.3.1 UART function mode

UART is a full-duplex asynchronous communication interface. The UART transceiver each contains a 16-byte FIFO buffer, and the user can set the receive cache trigger level, and can flexibly set the transmit byte length and stop bit length.

Support hardware automatic flow control function (CTS, RTS), and the trigger level of RTS flow control can be set, and the communication parameters of the full-duplex serial interface can be set.

3.9.3.2 UART interrupt and status

UART supports 9 types of interrupts, including the following:

- Receive interrupts after the threshold level reaches.
- Transmit FIFO empty interrupt.
- Line state interrupt (parity error, frame error, interruption interrupt).
- Modem status interrupt.
- Receive buffer timing overflow interrupt.
- Hardware flow interrupt (CTS/RTS).
- Software flow interrupt.

3.9.4 Register mapping

(UART0 base address = 0x4480_0000; UART1 base address = 0x4500_0000)

RO: read only; WO: write only; R/W: read and write

x is 0-1 in the following registers.

Register	Offset value	R/W	Description	Reset value
RBR	0x000	RO	Receive buffer register	-
THR	0x004	WO	Transmit buffer register	-
DLR	0x008	R/W	Baud rate divider register	0x01
IER	0x00c	R/W	Interrupt enable register	0x0
IIR	0x010	RO	Interrupt status register	0x01
FCR	0x014	WO	FIFO control register	0x0
LCR	0x018	R/W	Line control register	0x0
MCR	0x01C	R/W	Modem control register	0x0
LSR	0x020	RO	Line status register	0x60
MSR	0x024	RO	Modem status register	0x0
SCR	0x028	R/W	High-speed buffer register	0x0
EFR	0x02C	R/W	Advanced setting register	0x0
XON1	0x030	R/W	XON1 register	0x0
XON2	0x034	R/W	XON2 register	0x0
XOFF1	0x038	R/W	XOFF1 register	0x0
XOFF2	0x03C	R/W	XOFF2 register	0x0

3.9.5 Register description

3.9.5.1 Receive buffer register (RBR)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	RBR	Read, return the received data from the FIFO area	-

3.9.5.2 Transmit buffer register (THR)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	THR	Write data to the transmit buffer, the UART module will send the data at the top of the FIFO in order.	-

3.9.5.3 Baud rate divider register (DLR)

Bit	Symbol	Description	Reset value
31:16	-	Reserved	-
15:0	DLR	Baud rate = PCLK/16×DLR	0x1

3.9.5.4 Interrupt enable register (IER)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7	CTSIE	CTS interrupt enable bit (when AUTOIEN=1). 0: Disable 1: Enable	0x0
6	RTSIE	RTS interrupt enable bit (when AUTOIEN=1). 0: Disable 1: Enable	0x0
5	XOFIE	XOFF interrupt enable bit (when AUTOIEN=1). 0: Disable 1: Enable	0x0
4	-	Reserved	-
3	MDSIE	Modem status interrupt enable bit 0: Disable 1: Enable	0x0
2	RLSIE	Receive line status interrupt enable bit 0: Disable 1: Enable	0x0
1	THREIE	Transmit holding register empty interrupt enable bit 0: Disable 1: Enable	0x0
0	RBRIE	Receive data valid interrupt/receive timer overflow interrupt enable bit 0: Disable 1: Enable	0x0

3.9.5.5 Interrupt status register (IIR)

Bit	Symbol	Description	Reset value
31:6	-	Reserved	-
5	INTHFC	Hardware flow control status If the bit is 1, a rising edge is detected at the RTS or CTS pin and can be cleared by reading UARTxIIR	0x0
4	INTSFC	Software flow control status If the bit is 1, an XOFF character will be received. This bit can be cleared by reading the UARTxIIR	0x0
3:1	INTID	Interrupt status indication 0x0: Modem state changes 0x1: The transmit hold register is empty 0x2: The received data is valid 0x3: The line status is received 0x6: Receive timer overflow	0x0
0	INT STATUS	Interrupt status 0: At least one interrupt is in the queue 1: There is no interrupt in the queue	1

3.9.5.6 FIFO control register (FCR)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:6	RXTL	Receive trigger level, indicates how many bytes are received before the interrupt is triggered. 0x0: Level 0 (1 byte). 0x1: Level 1 (4 bytes). 0x2: Level 2 (8 bytes). 0x3: Level 3 (14 bytes).	0x0
5:4	TXTL	Transmit trigger level, indicates how many bytes to transmit before the interrupt is triggered. (when AUTOIEN=1) 0x0: Level 0 (N-1 bytes, N> = 1 is required, otherwise no interrupt will occur). 0x1: Level 1 (N-4 bytes, N> = 4 is required, otherwise there is no interrupt). 0x2: Level 2 (N-8 bytes, N> = 8 is required, otherwise no interrupt is generated). 0x3: Level 3 (N-14 bytes, N> = 14 is required, otherwise no interrupt is generated). Note: N is the number of bytes written to the FIFO, N< = 17.	0x0
3	-	Reserved	-
2	TXFIFO RST	Transmit FIFO reset Write 0: Unaffected 1: Clear all data from the transmit FIFO and reset the FIFO pointer. This bit is self-clearing.	0x0
1	RXFIFO RST	Receive FIFO reset Write 0: Unaffected 1: Clear all data from the transmit FIFO and reset the FIFO pointer. This bit is self-clearing.	0x0
0	FIFOEN	FIFOenable bit 0: Disable FIFO 1: Enable FIFO Note: When this bit is changed, all data in the transmit and receive FIFOs will be cleared automatically.	0x0

3.9.5.7 Line control register (LCR)

Bit	Symbol	Description	Reset value
31:7	-	Reserved	-
6	BCON	Break control bit When this bit is written to 1 to enable Break transmission, the TXD port will be forced to output a logic 0.	0x0
5:4	PSEL	Parity bit selection 0x0: Odd parity, the odd number of logic 1 is sent and detected in each byte 0x1: Even parity, the even number of logic 1 is sent and detected in each byte 0x2: The parity check bit is forced to be 1 0x3: The parity check bit is forced to be 0	0x0
3	PEN	Parity enable bit 0: Disable parity check bit generation and detection 1: Enable parity check bit generation and detection	0x0
2	SBS	Stop bit selection 0: 1-bit stop bit 1: When the transmit word length is 5 bits, the stop bit is 1.5 bits; when the transmit word length is other, the stop bit is 2 bits.	0x0
1:0	WLS	Word length selection bit 0x0: 5-bit 0x1: 6-bit 0x2: 7-bit 0x3: 8-bit	0x0

3.9.5.8 Modem control register (MCR)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7	XOFFS	XOFF status bit Read only 1: XOFF character received 0: XON character received	0x0
6	IREN	IrDA Modem enable bit 0: Disable 1: Enable	0x0
5	-	Reserved	-
4	MLBM	Modem loopback mode 0: Disable modem loopback mode 1: Enable modem loopback mode	0x0
3:2	-	Reserved	-
1	RTS	Modem mode RTS output bit 0: RTS output high 1: RTS output low When modem loopback mode is enabled, the bit is read as 0.	0x0
0	-	Reserved	-

3.9.5.9 Line status register (LSR)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7	RXFE	Receive FIFO error bit (read-only) This bit is set when a receive frame error, a checksum error, or an interrupt interrupt occurs. When there are no errors in the FIFO queue, this bit can be cleared by reading the LSR register.	0x0
6	TEMT	Transmit buffer empty flag bit (read-only) 0: Unfinished data in the transmit buffer 1: The transmit buffer is empty	1
5	THRE/FIFOE	When FIFOEN=0, it means the transmit register is empty (read-only). 0: Unfinished data in the transmit register 1: The transmit register is empty When FIFOEN=1, it means transmit FIFO empty flag bit (read-only). 0: Transmit FIFO has unsent data 1: Transmit FIFO is empty	1
4	BI	Interruption interrupt flag bit (read-only) 0: No interrupt detected 1: An interrupt detected When the UART data input remains low during a transmission (start bit, data, check digit, stop bit), an interruption interrupt is triggered. The UART remains idle until the data input is high. This bit can be cleared by reading the LSR register	0x0
3	FE	Frame error flag bit (read-only) 0: No frame error detected 1: A frame error detected This bit can be cleared by reading the LSR register.	0x0
2	PE	Parity check error flag bit (read-only) 0: Parity check error not detected 1: Parity check error detected This bit can be cleared by reading the LSR register.	0x0
1	OE	FIFO overflow error flag bit (read-only) 0: No FIFO overflow error detected 1: A FIFO overflow error is detected A FIFO overflow error occurs when the FIFO is full and new data is received, in which case the data in the FIFO is not rewritten, but the newly received data is lost. This bit can be cleared by reading the LSR register.	0x0
0	RDR	Receive data valid flag bit (read-only) 0: No unread data in the receive area 1: There is unread data in the receive area.	0x0

3.9.5.10 Modem status register (MSR)

Bit	Symbol	Description	Reset value
31:5	-	Reserved	-
4	CTS	CTS pin status (read-only) 0: The CTS pin input status is low 1: The CTS pin input status is high When moden loopback mode is enabled, the CTS pin status is connected to the MCR[1].	0x0
3:1	-	Reserved	-
0	DCTS	Detect CTS pin level change flag bit (read-only) 0: No level change on CTS input pin 1: Level change on CTS input pin This bit can be cleared by reading the MSR register	0x0

3.9.5.11 High-speed buffer register (SCR)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	PAD	Readable/writable 8-bit register	0x0

3.9.5.12 Advanced setting register (UARTxEFR)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7	AUTOCTS	Hardware transmit flow control 0: Disable 1: Enable	0x0
6	AUTORTS	Hardware receive flow control 0: Disable 1: Enable	0x0
5	-	Reserved	-
4	AUTOIEN	Flow control interrupt enable 0: Disable 1: Enable (Control CTSIE, RTSIE, XOFIE write enable)	0x0
3:2	TXSWFC	Transmit software flow control bit 0x0: Disable transmitting software flow control 0x1: Transmit XON1/XOFF1 as flow control characters 0x2: Transmit XON2/XOFF2 as flow control characters 0x3: Transmit XON1 & XON2 and XOFF1 & XOFF2 as flow control characters	0x0
1:0	RXSWFC	Receive software flow control bit 0x0: Disable receiving software flow control 0x1: Receive XON1/XOFF1 as flow control characters 0x2: Receive XON2/XOFF2 as flow control characters 0x3: Receive XON1 & XON2 and XOFF1 & XOFF2 as flow control characters	0x0

3.9.5.13 XON1, XON2 registers (XON1/XON2)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	HXON	XON character	0x0

3.9.5.14 XOFF1, XOFF2 registers (XOFF1/XOFF2)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	HXOFF	XOFF character	0x0

3.10 I²C Serial interface controller (I²C)

3.10.1 Overview

I²C is a two-wire bidirectional serial bus that provides a simple and efficient connection for data exchange between devices. I²C is a true multi-master bus that incorporates conflict detection and arbitration mechanisms. Conflict detection and arbitration mechanisms are used to prevent data corruption in cases where two or more hosts are simultaneously trying to control the bus.

3.10.2 Features

- Support master/slave mode.
- Bidirectional data transfer between master and slave.
- Multi-master bus.
- Simultaneous data arbitration between multiple hosts to avoid serial data corruption on the bus.
- The bus uses a serial synchronous clock that enables different rates between devices.
- Serial synchronous clocks can be used as a handshake mechanism to implement suspend and resume serial transmissions.
- Programmable clocks can be used for a variety of rate controls.
- Support 7-bit/10-bit slave address modes.
- Support multi-address recognition (4 groups of slave addresses with mask option).
- Support wake-up mode.

3.10.3 Feature description

3.10.4 Register mapping

(I2C0 base address = 0x4800_0000) RO: read only; WO: write only; R/W: read and write.

Register	Offset value	R/W	Description	Reset value
CONSET	0x000	R/W	I²C control set register	0x0
CONCLR	0x004	WO	I²C control clear register	0x0
STAT	0x008	RO	I²C status register	0Xf8
DAT	0x00C	R/W	I²C data register	0x0
CLK	0x010	R/W	I²C clock control registers	0x0
ADR0	0x014	R/W	I²C slave address register 0	0x0
ADM0	0x018	R/W	I²C slave address mask register 0	0Xfe
XADR0	0x01C	R/W	I²C extended slave address register 0	0x0
XADM0	0x020	R/W	I²C extended slave address mask register 0	0x1FE
RST	0x024	WO	I²C software reset registers	0x0
ADR1	0x028	R/W	I²C slave address register 1	0x0
ADM1	0x02C	R/W	I²C slave address mask register 1	0Xfe
ADR2	0x030	R/W	I²C slave address register 2	0x0
ADM2	0x034	R/W	I²C slave address mask register 2	0Xfe
ADR3	0x038	R/W	I²C slave address register 3	0x0
ADM3	0x03C	R/W	I²C slave address mask register 3	0Xfe

3.10.5 Register description

3.10.5.1 I²C control set register (CONSET)

Bit	Symbol	Description	Reset value
31:9	-	Reserved	-
8	GCF	I²C broadcast call flag bit Read only 0: No broadcast call received 1: Broadcast call address matching This bit is cleared when new data is received or sent	0x0
7	I2CIE	Interrupt enable bit 0: Disable 1: Enable	0x0
6	I2CEN	I²C interface enable bit 0: Disable the I²C interface 1: Enable the I²C interface Note: Enable the I²C interface by writing a 1 to the I2CEN bit, disable the I²C interface by writing a 1 to the I2CENC bit (I2CxCONCLR).	0x0
5	STA	Start flag bit Write 1, I2C switches to master mode and transmits a start signal; - When I²C is already in master mode, a restart signal is transmitted. - When I²C is in slave mode, write 1 ends the current transfer and waits for the bus to become idle to enter master mode. Writing 0 does not affect it. - This bit is automatically cleared when the start bit or restart bit is sent.	0x0
4	STO	Stop flag bit When writing 1 in master mode, a stop bit is sent. When writing 1 in slave mode, the I²C module treats it as if it received a stop bit. - When STA and STO are set at the same time, the I²C module sends a stop bit followed by a start bit. - This bit is automatically cleared when the stop bit is sent.	0x0
3	SI	I²C interrupt flag bit Read only This bit can be cleared by writing 1 to the SIC bit when the I²C bus state changes.	0x0
2	AA	ACK flag bit 0: No ACK signal received 1: Response to the ACK signal in the following cases ● When slave address is matched ● When a broadcast call is enabled and a broadcast address is received ● This bit can be cleared by writing a 1 to the AAC bit when data is received in master or slave mode	0x0
1	XADRF	I²C slave 10-bit address flag bit Read only 0: I²C address mismatch 1: 1²C 10-bit address match This bit is cleared when new data is sent or received	0x0
0	ADRF	I²C slave 7-bit address flag bit Read only 0: I²C address mismatch 1: 1²C 7-bit address match This bit is cleared when new data is sent or received	0x0

3.10.5.2 I²C control clear register (CONCLR)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7	I2CIEC	I²C interrupt disable bit Write 1 to clear the I2CIE bit Writing 0 does not affect	0x0
6	I2CENC	I²C interface disable bit Write 1 to clear the I2CEN bit Writing 0 does not affect	0x0
5	STAC	Start flag clear bit Write 1 to clear the STA bit Writing 0 does not affect	0x0
4	-	Reserved	-
3	SIC	I²C interrupt flag clear bit Write 1 to clear the SI bit Writing 0 does not affect	0x0
2	AAC	I²C ACK flag clear bit Write 1 to clear the AA bit Writing 0 does not affect	0x0
1:0	-	Reserved	-

I2C operation requires clearing the corresponding flag bit to proceed to the next state.

3.10.5.3 I²C status register (STAT)

Bit	Symbol	Description		Reset value
31:8	-	Reserved		-
7:0	Status	I²C status code		0Xf8
		00h	Bus error (valid only in master mode)	
		08h	Start bit transmit completion	
		10h	Restart bit transmit completion	
		18h	Address + write bit transmit completion and the ACK is received	
		20h	Address + write bit transmit completion, and the ACK is not received	
		28h	In master mode, the data transmission is completed and the ACK is received	
		30h	In master mode, the data transmission is completed and the ACK is not received	
		38h	Arbitration fails during address or data transfer	
		40h	Address + read bit transmit completion, and the ACK is received	
		48h	Address + read bit transmit completion, and the ACK is not received	
		50h	Received data in master mode with ACK response	
		58h	Received data in master mode without ACK response	
		60h	Receive address + write bit in slave mode with ACK response	
		68h	Master arbitration failed, receive slave address + write bit with ACK response	
		70h	Received broadcast call address with ACK response	
		78h	Master arbitration failed, received broadcast call address with ACK response	
		80h	Received data after slave address match with ACK response	
		88h	Received data after slave address match without ACK response	
		90h	Receive data after slave receives broadcast call address with ACK response	
		98h	Receive data after slave receives broadcast call address without ACK response	
		A0h	Receive stop signal or restart signal in slave mode.	
		A8h	Receive address + read bit in slave mode with ACK response	
		B0h	Master arbitration failure, receive slave address + read bit with ACK response	
		B8h	Receive an ACK after sending data in slave mode.	
		C0h	Received no ACK after sending data in slave mode.	
		C8h	Received an ACK after sending the last data in slave mode.	
		D0h	After sending the last data in slave mode, ACK is not received.	
		D8h	Not used	
		E0h	Received an ACK after sending the second address in host mode.	
		E8h	Second address sent in host mode, no ACK received.	
		F0h	Not used	
		F8h	Undefined state	
		Other	Reserved	

3.10.5.4 I²C data register (DAT)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	Data	Data received or to be sent	0x0

3.10.5.5 I²C clock control register (CLK)

Bit	Symbol	Description	Reset value
31:7	-	Reserved	-
6:4	M	Sample clock = PCLK/2^M	0x0
3:0	N	SCL clock= PCLK/ (2^M× (N+1)×10)	0x0

3.10.5.6 I²C slave address register (ADR0/ADR1/ADR2/ADR3)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:1	Address	Slave address	0x0
0	GC	1: Enable broadcast call address recognition 0: Disable broadcast call address recognition	0x0

3.10.5.7 I²C slave address mask register (ADM0/ADM1/ADM2/ADM3)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:1	MASK	Mask bit 0: The bit address is not compared 1: Compare the address of this bit	0x7F
0	-	Reserved	-

3.10.5.8 I²C extended slave address register (XADR0)

Bit	Symbol	Description	Reset value
31:11	-	Reserved	-
10:1	Address	10-bit slave address	0x0
0	GC	1: Enable broadcast call address recognition 0: Disable broadcast call address recognition	0x0

3.10.5.9 I²C extended slave address mask register (XADM0)

Bit	Symbol	Description	Reset value
31:9	-	Reserved	-
8:1	MASK	Mask bit 0: The bit address is not compared 1: Compare the address of this bit	0Xff
0	-	Reserved	-

3.10.5.10 I²C software reset register (RST)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	RST	Writes 0x07, resulting in a software reset	0x0

3.11 Serial peripheral interface controller (SSP/SPI)

3.11.1 Overview

Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol that operates in full-duplex mode. The devices can operate in master/slave mode, communicating with each other using a 4-wire bidirectional interface. When receiving data from a peripheral device, SPI performs a serial-to-parallel conversion, and when the data is sent to the peripheral, it performs a parallel-to-serial conversion. The SPI controller can be configured as either a master or a slave.

3.11.2 Features

- Support master or slave mode.
- Full duplex.
- The transmit bit length can be configured.
- MSB first transmission/reception.
- 8x 16-bit transmit/receive FIFOs.

3.11.3 Register mapping

(SSP0 base address= 0x4380_0000) RO: read only; WO: write only; R/W: read and write.

Register	Offset value	R/W	Description	Reset value
CON	0x000	R/W	SSP control register	0x0
STAT	0x004	RO	SSP status register	0x3
DAT	0x008	R/W	SSP data register	0x0
CLK	0x00C	R/W	SSP clock control register	0x0
IMSC	0x010	R/W	SSP interrupt enable register	0x0
RIS	0x014	RO	SSP interrupt source status register	0x8
MIS	0x018	RO	SSP enabled interrupt status register	0x0
ICLR	0x01C	WO	SSP interrupt clear register	0x0
CSCR	0x028	R/W	SSP software chip select signal register	0x0

3.11.4 Register description

3.11.4.1 SSP control register (CON)

Bit	Symbol	Description	Reset value
31:12	-	Reserved	-
11	LBM	Loopback mode enable bit 0: Normal working mode 1: Loopback mode, serial input to serial output	0x0
10	SSPEN	SSP enable bit 0: Disable 1: Enable	0x0
9	MS	Master/slave mode select bit 0: Master mode 1: Slave mode	0x0
8	SOD	Slave output disable bit valid only in slave mode 0: SSP can output MISO 1: SSP can not output MISO	0x0
7	CPH	Clock phase control bit 0: SSP samples data on the first clock edge 1: SSP samples data on the second clock edge	0x0
6	CPO	Clock output polarity select bit 0: SPI_CLK is low when idle 1: SPI_CLK is high when idle	0x0
5:4	FRF	Frame format 0x0: SPI- compatible frame format 0x1: TISS- compatible frame format 0x2: Microwire - compatible frame format 0x3: Reserved	0x0
3:0	DSS	Data transfer length select bit 0x0: Reserved 0x1: Reserved 0x2: Reserved 0x3: 4 bits 0x4: 5 bits 0x5: 6 bits 0x6: 7 bits 0x7: 8 bits 0x8: 9 bits 0x9: 10 bits 0Xa: 11 bits 0Xb: 12 bits 0Xc: 13 bits 0Xd: 14 bits 0Xe: 15 bits 0Xf: 16 bits	0x0

3.11.4.2 SSP status register (STAT)

Bit	Symbol	Description	Reset value
31:5	-	Reserved	-
4	BSY	Busy flag bit Read-only 0: SSP idle 1: SSP is transmitting/receiving data or transmit FIFO is not empty	0x0
3	RFF	Receive FIFO full flag bit Read-only 0: Receiving FIFO is not full 1: Receiving FIFO is full	0x0
2	RNE	Receive FIFO non-empty flag bit Read-only 0: The receive FIFO is empty 1: The receive FIFO is not empty	0x0
1	TNF	Transmit FIFO not full flag bit Read-only 0: Transmit FIFO is full 1: Transmit FIFO not full	0x1
0	TFE	Transmit FIFO empty flag bit Read-only 0: Transmit FIFO is not empty 1: Transmit FIFO is empty	0x1

3.11.4.3 SSP data register (DAT)

Bit	Symbol	Description	Reset value
31:16	-	Reserved	-
15:0	DATA	Write data to this register, when there is no data on the bus in the send, the data will be sent out immediately; When there is data on the bus that is being sent, the data is stored in the FIFO and sent sequentially. The minimum interval between send times is 3 SSPCLK clocks. When the data length is less than 16 bits, it needs to be right-aligned. Read this register, read the most recently received data, when the data length is less than 16 bits, need to be right-aligned.	0x0

3.11.4.4 SSP clock controller (CLK)

Bit	Symbol	Description	Reset value
31:16	-	Reserved	-
15:8	M	SSPCLK = PCLK / ((M+1)×N)	0x0
7:0	N	N is an even number in the range 2-254	0x0

3.11.4.5 SSP interrupt enable register (IMSC)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3	TXIM	Transmit FIFO interrupt enable bit 0: Disable transmitting FIFO half-empty interrupts 1: Enable transmitting FIFO half-empty interrupts	0x0
2	RXIM	Receive FIFO interrupt enable bit 0: Disable receiving FIFO half-full interrupts 1: Enable receiving FIFO half-full interrupts	0x0
1	RTIM	Receive FIFO timer overflow interrupt enable bit 0: Disable receiving FIFO timer overflow interrupts 1: Enable receiving FIFO timer overflow interrupts (Overflow time: 64×SSPCLK).	0x0
0	RORIM	Receive FIFO overflow interrupt enable bit 0: Disable receiving FIFO overflow interrupts 1: Enable receiving FIFO overflow interrupts	0x0

3.11.4.6 SSP interrupt source status register (RIS)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3	TXRIS	This bit is set when the transmit FIFO is at least half-empty (automatically cleared if it is not half-empty).	0x1
2	RXRIS	This bit is set when the receive FIFO is at least half-full (automatically cleared if it is not half-full).	0x0
1	RTRIS	This bit is set when the receive FIFO is not empty and the timeout period has elapsed without being read.	0x0
0	RORRIS	When the receive FIFO is full and another frame is received, this bit is set and the old data will be lost.	0x0

3.11.4.7 SSP enabled interrupt status register (MIS)

Bit	Symbol	Description	Reset value
31:4	-	Reserved	-
3	TXMIS	This bit is set when the transmit FIFO half-empty interrupt is enabled and the transmit FIFO is at least half-empty.	0x0
2	RXMIS	This bit is set when the receive FIFO half-full interrupt is enabled and the receive FIFO is at least half-full.	0x0
1	RTMIS	This bit is set when the receive FIFO timer overflow interrupt is enabled, and the receive FIFO is not empty and has not been read after the timeout period.	0x0
0	RORMIS	This bit is set when the receive FIFO timer overflow interrupt is enabled, the receive FIFO is full, and a frame is received.	0x0

3.11.4.8 SSP interrupt clear register (ICLR)

Bit	Symbol	Description	Reset value
31:2	-	Reserved	-
1	RTIC	Write 1 to clear the RTRIS flag bit	0x0
0	RORIC	Write 1 to clear the RORRIS flag bit	0x0

3.11.4.9 SSP software chip select signal register (CSCR)

Bit	Symbol	Description	Reset value
31:5	-	Reserved	-
4	SPH	Slave chip select signal 0: After each frame of data transmission is completed, the chip selection signal cannot be pulled high 1: After each frame of data transmission is completed, the chip selection signal must be pulled high	0x0
3	SWCS	Software chip select signal control bit in master mode 0: Output low 1: Output high	0x0
2	SWSEL	Select signal selection in master mode 0: The chip selection signal is automatically controlled by the SPI module 1: The chip selection signal is controlled by the SWCS bit	0x0
1:0	-	Reserved	-

3.12 Fast analog-to-digital conversion (ADC1)

3.12.1 Overview

The chip contains a 12-bit, 30-channel successive approximation analog-to-digital converter (ADC1).

3.12.2 Features

- Analog input voltage range: 0 ~ AVDD
- 12-bit resolution 10-bit valid guarantee
- Up to 30 single-ended analog input channels.
- Up to 1.4Msps conversion rate (including sampling ->conversion time)
- Up to 1.2Msps continuous mode conversion rate (including start ->sampling ->conversion time)
- Two modes of operation
  Single-shot mode: Performs an A/D conversion on the specified channel.
  Continuous mode: A/D conversion is performed on all selected channels.
- The conversion results for each channel are stored in the corresponding data registers.
- The fastest time for a single AD conversion is about 0.8us
- The total time for AD conversion of any four channels in continuous mode is about 3.2us
- Under continuous mode, the total time of AD conversion of 16 channels can be completed as soon as 12.8us
- Channel 30 can be used to test internal analog voltage signals (Including op amp output/internal 1.2V reference voltage)

3.12.3 Feature description

3.12.3.1 ADC channel

ADC channel number	ADC channel	Description
0	AN0	ADC channel 0
1	AN1	ADC channel 1
2	AN2	ADC channel 2
…	…	…
n	Ann	ADC channel n
…	…	…
29	AN29	ADC channel 29
30	AN30	Internal analog channel

Note: Any combination of AN0-AN30 channels supports continuous mode switching.

AN30 channel internal analog selection:

ADCICHS<2:0>	Internal analog selection	Description
0	Bandgap(1.2V)	1.2V reference source
1	OP0_OUT	Output of OP0
2	OP1_OUT	Output of OP1
3	PGA0_OUT	Output of PGA0
4	PGA1_OUT	Output of PGA1
5	VSS	Negative reference voltage
6	VDD	Positive reference voltage
7	VSS	Negative reference voltage

3.12.3.2 ADC calibration

Before the ADC measures the analog voltage, it is recommended that the ADC module to be calibrated for higher performance and resolution. The calibration method is as follows:

1) Set the speed and sample-and-hold time of the ADC's internal comparator
2) Set the clock division of the ADC
3) Turn on the enable bit of the ADC
4) Turn on the calibration enable bit ADCCALEN for the ADC
5) After the calibration is completed, the ADCCALEN hardware is automatically cleared and the calibration process is completed

Calibration time approx.: $4096 \times T_{ADC}$ (T_{ADC} is the conversion clock of the ADC).

After calibration, initiate normal ADC conversion, keep ADCALCONV=0, and enable ADC conversion operation with calibration data.

3.12.3.3 ADC software start

Writing 1 in register ADCCON2.ADCST bit initiates the ADC conversion. After the conversion is complete, the bit hardware is automatically cleared to zero.

During an ADC conversion, any software and hardware triggering start signals are ignored.

3.12.3.4 ADC hardware trigger start

Trigger source:

In addition to software-initiated conversions, the ADC can be externally triggered by a hardware trigger for ADC conversions.

External trigger:

The external trigger can be selected from rising edge or falling edge to start the ADC, after detecting the external trigger signal, ADCST will be set to 1 to start the ADC conversion after 2 PCLK clock filtering.

3.12.4 Register mapping

(ADC1 base address = 0x4D80_0000) RO: read-only; WO: write only; R/W: read and write

Register	Offset value	R/W	Description	Reset value
CON(P1B)	0x000	R/W	ADC control register	0x0
CON2(P1B)	0x004	R/W	ADC control register 2	0x0
HWTG(P1B)	0x008	R/W	ADC hardware trigger control register	0x0
-	0x00C	-	Reserved	-
SCAN(P1B)	0x010	R/W	ADC scan register	0x0
CMP0(P1B)	0x014	R/W	ADC comparator 0 control register	0x0
-	0x018	-	Reserved	-
IMSC(P1B)	0x01C	R/W	ADC interrupt enable register	0x0
RIS	0x020	RO	ADC interrupt source status register	0x0
MIS	0x024	RO	ADC enabled interrupt status register	0x0
ICLR	0x028	WO	ADC interrupt clear register	0x0
LOCK	0x02C	R/W	ADC write enable control register	0x0
-	0x030	-	Reserved	-
-	0x034	-	Reserved	-
-	0x038	-	Reserved	-
-	-	-	-	-
DATA0	0x080	RO	ADC channel 0 conversion result register	0x0
DATA1	0x084	RO	ADC channel 1 conversion result register	0x0
DATA2	0x088	RO	ADC channel 2 conversion result register	0x0
DATA3	0x08C	RO	ADC channel 3 conversion result register	0x0
DATA4	0x090	RO	ADC channel 4 conversion result register	0x0
DATA5	0x094	RO	ADC channel 5 conversion result register	0x0
DATA6	0x098	RO	ADC channel 6 conversion result register	0x0
DATA7	0x09C	RO	ADC channel 7 conversion result register	0x0
DATA8	0x0A0	RO	ADC channel 8 conversion result register	0x0
DATA9	0x0A4	RO	ADC channel 9 conversion result register	0x0
DATA10	0x0A8	RO	ADC channel 10 conversion result register	0x0
DATA11	0x0AC	RO	ADC channel 11 conversion result register	0x0
DATA12	0x0B0	RO	ADC channel 12 conversion result register	0x0
DATA13	0x0B4	RO	ADC channel 13 conversion result register	0x0
DATA14	0x0B8	RO	ADC channel 14 conversion result register	0x0
DATA15	0x0BC	RO	ADC channel 15 conversion result register	0x0
DATA16	0x0C0	RO	ADC channel 16 conversion result register	0x0
DATA17	0x0C4	RO	ADC channel 17 conversion result register	0x0
DATA18	0x0C8	RO	ADC channel 18 conversion result register	0x0
DATA19	0x0CC	RO	ADC channel 19 conversion result register	0x0
DATA20	0x0D0	RO	ADC channel 20 conversion result register	0x0
DATA21	0x0D4	RO	ADC channel 21 conversion result register	0x0
DATA22	0x0D8	RO	ADC channel 22 conversion result register	0x0
DATA23	0x0DC	RO	ADC channel 23 conversion result register	0x0

DATA24	0x0E0	RO	ADC channel 24 conversion result register	0x0
DATA25	0x0E4	RO	ADC channel 25 conversion result register	0x0
DATA26	0x0E8	RO	ADC channel 26 conversion result register	0x0
DATA27	0x0EC	RO	ADC channel 27 conversion result register	0x0
DATA28	0x0F0	RO	ADC channel 28 conversion result register	0x0
DATA29	0x0F4	RO	ADC channel 29 conversion result register	0x0
DATA30	0x0F8	RO	ADC channel 30 conversion result register	0x0

Note: The registers marked (P1B) are protected registers.

(P1B): When LOCK=55H, the labeled register is allowed to write; = Other values, forbidden to write.

3.12.5 Register description

3.12.5.1 ADC control register (CON)

Bit	Symbol	Description	Reset value
31	ADCRST	ADC module reset control bit 0: - 1: ADC module reset	0x0
30:26	-	Reserved	-
25	ADCCONVER	ADC conversion error flag bit 0: - 1: ADC conversion error	0x0
24	ADCCALERR	ADC calibration error flag bit 0: - 1: ADC calibration error	0x0
23:22	-	Reserved	-
21	ADCCONVERRCLR	ADC conversion error flag clear bit 0: - 1: Clear the ADCCONVERR bit	0x0
20	ADCCALERRCLR	ADC calibration error flag clear bit 0: - 1: Clear the ADCCONVERR bit	0x0
19	-	Reserved	-
18:16	ADCICHS	ADC internal analog selection (connected to channel AN30) 000: Bandgap 001: OP0_OUT 010: OP1_OUT 011: PGA0_OUT 100: PGA1_OUT 101: VSS (ADC reference negative) 110: VDD (ADC reference positive) 111: VSS	0x0
15	-	Reserved	-
14	ADCSS	ADC internal comparator speed select bit 0: Support FADC up to 32MHz 1: Support FADC up to 4MHz	0x0
13:12	ADCSHT	ADC sample-and-hold time selection bit 00: 3.5 ADC clock cycles 01: 4.5 ADC clock cycles 10: 6.5 ADC clock cycles 11: 10.5 ADC clock cycles	0x0
11:5	-	Set to 0	-
4	ADCEN	ADC enable control bit 0: Disable 1: Enable	0x0
3	ADCMS	ADC mode selection bit 0: Single conversion 1: Continuous conversion (Convert all enabled ADC channels at	0x0

		once)	
2:0	ADCDIV	ADC clock prescaler selection bit $F_{ADC} = PCLK/2^{ADCDIV}$	0x0

3.12.5.2 ADC control register 2 (CON2)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7	ADCST	ADC conversion start (hardware is automatically cleared to zero out after conversion) 0: The conversion is over or the ADC is in idle mode (Invalid to write 0) 1: Start the conversion (ADCEN must be 1)	0x0
6:2	-	Reserved	-
1	ADCCALCONV	ADC calibration function enable bit 0: Enable ADC conversion with calibration data 1: Disable	0x0
0	ADCCALEN	ADC calibration enable bit 0: - (Invalid to write 0) 1: Enable (auto cleared after calibration is completed)	0x0

The calibration time is approximately 4096×T_{ADC} (T_{ADC} is the conversion clock of the ADC).

3.12.5.3 ADC hardware trigger control register (HWTG)

Bit	Symbol	Description	Reset value
31:18	-	Reserved	-
17	ADCEXTEN	ADC external trigger enable bit 0: Disable 1: Enable	0x0
16	ADCEXTES	ADC external trigger edge selection bit 0: Falling edge 1: Rising edge	0x0
15:0	-	Reserved	-

3.12.5.4 ADC scan register (SCAN)

Bit	Symbol	Description	Reset value
31	-	Reserved	-
30:0	ADCEn	ADC channel n enable bit (n=30-0) 0: Disable 1: Enable	0x0

3.12.5.5 ADC conversion result register (DATAx) x=0-30

Bit	Symbol	Description	Reset value
31:12	-	Reserved	-
11:0	RSLT	ADC conversion result	0x0

3.12.5.6 ADC comparison control register 0(CMP0)

Bit	Symbol	Description	Reset value
31	ADCCMP0EN	ADC comparator 0 enable bit 0: - 1: Enable	0x0
30	ADCCMP0O	ADC comparator 0 result bit (read only) (The selected channel is automatically updated after the conversion is completed) 0: Comparison conditions are not satisfied 1: Satisfying the conditions for comparison	0x0
29	-	Reserved	-
28	ADCCMP0COND	ADC comparator 0 compare condition select bit 0: ADC results < preset value 1: ADC result > = preset value	0x0
27:24	ADCCMP0MCNT	ADC comparator 0 match count preset value When the analog-to-digital conversion result of the specified channel matches the comparison condition, the internal counter is incremented by 1. When the internal counter equals the value of ADCCMP0MCNT+1, the internal counter value is cleared to zero automatically afterwards. Generate ADC compare event while matching Caution: The ADC Comparator 0 compare event will set the interrupt flag ADCCMP0IF to 1;	0x0
23:21	-	Reserved	-
20:16	ADCCMP0CHS	ADC comparator 0 compare channel select bit 00000- Channel 0 .... 11110- Channel 30	0x0
15:12	-	Reserved	-
11:0	ADCCMP0DATA	ADC comparator 0 data preset value (12 bits)	0x0

3.12.5.7 ADC interrupt enable register (IMSC)

Bit	Symbol	Description	Reset value
31	ADCIMSC31	ADC comparator 0 interrupt enable bit 0: Disable 1: Enable	0x0
30:0	ADCIMSCn	ADC channel n interrupt enable bit (n=30-0) 0: Disable 1: Enable	0x0

3.12.5.8 ADC interrupt source status register (RIS)

Bit	Symbol	Description	Reset value
31	ADCRIS31	ADC comparator 0 interrupt source state 0: No interrupt generated by interrupt source 1: Interrupt generated by interrupt source	0x0
30:0	ADCRISn	ADC channel n interrupt source state (n=30-0) 0: No interrupt generated by interrupt source 1: Interrupt generated by interrupt source	0x0

3.12.5.9 ADC enabled interrupt status register (MIS)

Bit	Symbol	Description	Reset value
31	ADCMIS31	ADC comparator 0 interrupt state 0: No interruptions generated 1: Enable and generate interrupt	0x0
30:0	ADCMISn	ADC channel n interrupt state (n=30-0) 0: No interruptions generated 1: Enable and generate interrupt	0x0

3.12.5.10 ADC interrupt clear register (ICLR)

Bit	Symbol	Description	Reset value
31	ADCICLR31	Write 1 to clear ADC comparator 0 interrupt state Writing 0 does not affect	0x0
30:0	ADCICLRn	Write 1 to clear ADC channel n interrupt state Writing 0 does not affect (n=30-0)	0x0

3.12.5.11 ADC write enable control register (LOCK)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	LOCK	When LOCK=0x55, enable the operation of ADC related registers. (See ADC Register mapping for details) When LOCK=other value, the operation of ADC related registers is prohibited.	0x0

3.13 Operational Amplifier (OP0/1, PGA0/1)

3.13.1 Overview

The chip contains two basic op-amp blocks and two programmable gain amplifiers. A small number of peripheral components can be used to achieve basic signal amplification and signal calculation functions.

3.13.2 Features

OP (Operational Amplifier)

- Each op-amp is multiplexed on all three ends with the GPIO port.
- Configurable to comparator mode.
- The op amp output can be internally connected to ADC channel 30 for measurement.

PGA (Programmable Gain Amplifier)

- Adjustable gain: 4X/8X/10X/12X/14X/16X/32X
- The PGA output can be internally connected to ADC channel 30 for measurement.

3.13.3 Function description

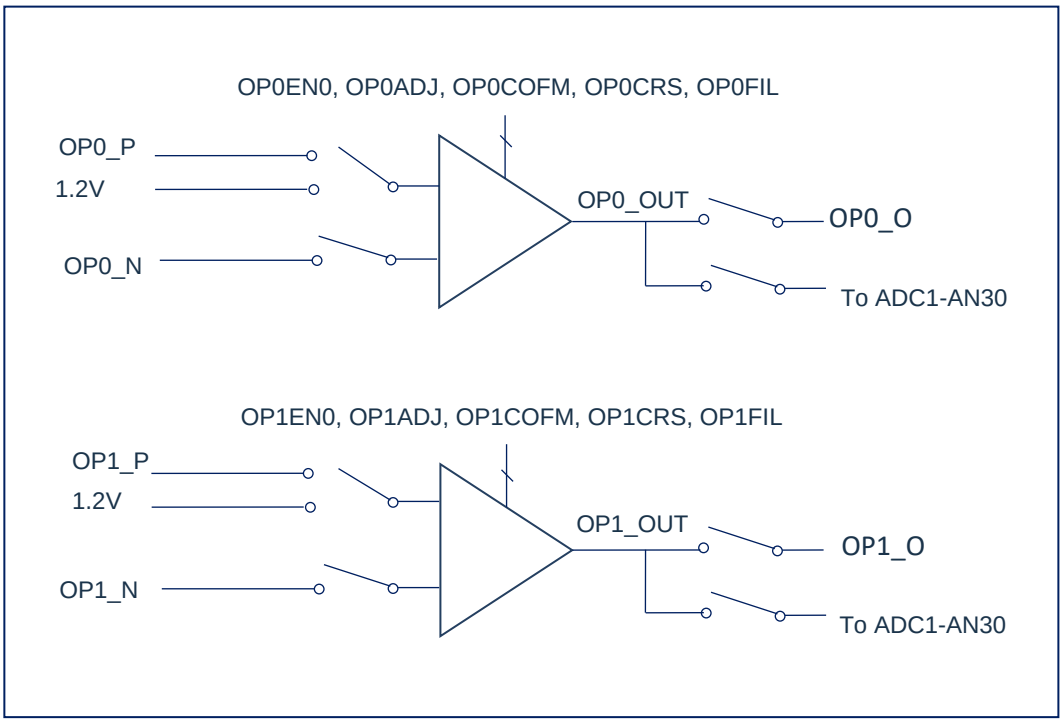


Figure 3-10: Op Amp vs. PGA structure diagram (1)

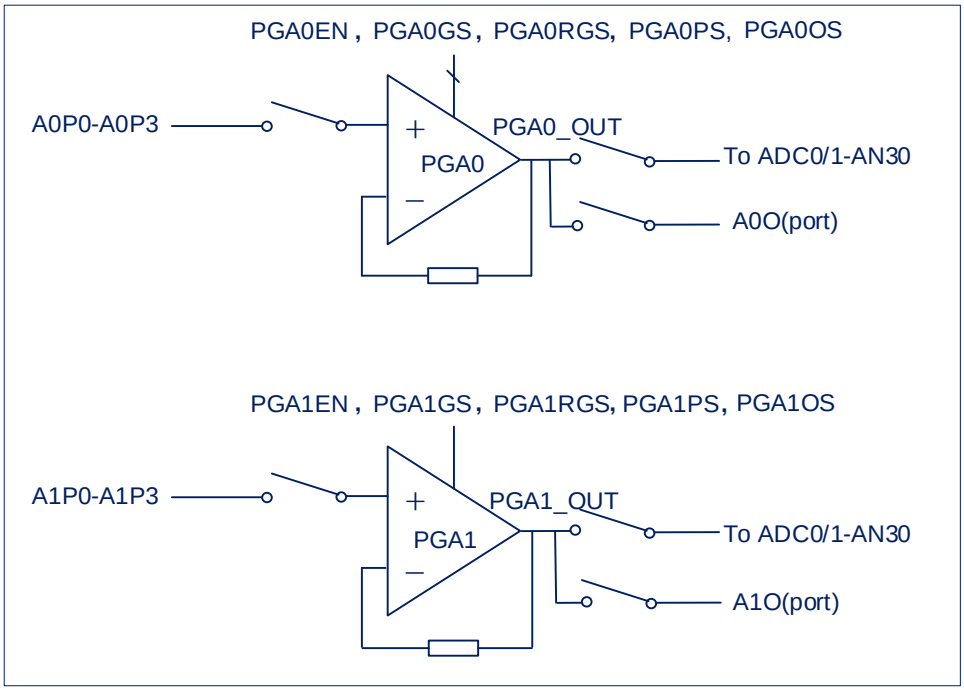


Figure 3-11: Op Amp vs. PGA structure diagram (2)

3.13.4 Register mapping

(OP0 base address = 0x4C80_0000; OP1 base address = 0x4C80_000C)

RO: read only, WO: write only, R/W: both read and write

Register	Offset value	R/W	Description	Reset value
CON0	0x000	R/W	OP control register 0	0x0
CON1	0x004	R/W	OP control register 1	0x10

(PGA0 base address = 0x4C80_0018; PGA1 base address = 0x4C80_0024)

RO: read only, WO: write only, R/W: both read and write

Register	Offset value	R/W	Description	Reset value
CON	0x000	R/W	PGA control register	0x0

3.13.5 Register description

3.13.5.1 Op Amp n control register 0 (CON0)(n=0-1)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7	OpnEN	Op amp n enable bit 0: Disable 1: Enable	0x0
6	OPnCOFM	Op amp n mode enable bit 0: Disable 1: Enable	0x0
5	OPnFIL	Op amp n operating mode selection 0: Op amp mode (OPnCOFM must be 0). 1: Comparison mode (OPnCOFM must be 0).	0x0
4	OpnOS	p amp n output channel enable bit 0: Disable 1: OPn_O output enable	0x0
3:2	OpnNS	Op amp n negative channel selection bit 00: Opn_N Other: Disable	0x0
1:0	OpnPS	Op amp n positive channel selection bit 00: Opn_P 01: 1.2V(Bandgap) Other: Disable	0x0

3.13.5.2 Op Amp n control register 1(CON1)(n=0-1)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7	OPnOUT	Op amp n adjusts the resulting bit/comparator mode output (read-only)	0x0
6	OPnCRS	Op amp n mode input select bit 0: Negative input 1: Positive input	0x0
5:0	-	Reserved	-

3.13.5.3 PGAn control register (CON)(n=0-1)

Bit	Symbol	Description	Reset value
31:16	-	Reserved	-
15	PGAnEN	PGAn enable bit 0: Disable 1: Enable (PGA0EN must also be 1 if only PGA1 is used).	0x0
14:12	PGAnGS	PGAn gain select bit 000: 4x 001: 8x 010: 10x 011: 12x 100: 14x 101: 16x 11x: 32x	0x0
11	PGAnRGS	PGAn feedback resistor ground selection 0: The ground connected to the module 1: Connect to the dedicated ground wire PIN	0x0
10	-	Reserved	-
9:8	PGAnOS	PGAnutput channel enable bit 00: Disable 01: AnO output enabled 1x: Disable	0x0
7:4	PGAnPS	PGAn positive channel selection bit 00: AnP0 01: AnP1 10: AnP2 11: AnP3	0x0
3:0	-	Reserved	-

3.14 Analog comparator (ACMP0/1)

3.14.1 Overview

Inside the chip are two analog comparators. The comparator can be configured for different applications. When the positive voltage is greater than the negative voltage, the comparator outputs logic 1 and vice versa output 0, which can also be changed by the output polarity select bit. When the comparator output value changes, each comparator can be configured to generate an interrupt.

3.14.2 Features

- Analog input voltage range: 0 ~ (VDD-1.5V).
- Hysteresis voltage selection (10mV/20mV/60mV-typ) is supported.
- Each comparator positive terminal can select 4 port inputs.
- Each comparator negative terminal can select the port input and internal reference voltage.
- The internal reference voltage VREF selects the divider output of the internal Bandgap (1.2V) and VDD.
- Internal reference voltage divider range: (2/20) $\times V_{REF}$ to (17/20) $\times V_{REF}$ with a total of 16 gears.
- Output filterable time can be selected: (0 to 512)× Tsys.
- Output changes can produce interrupts.

3.14.3 Function description

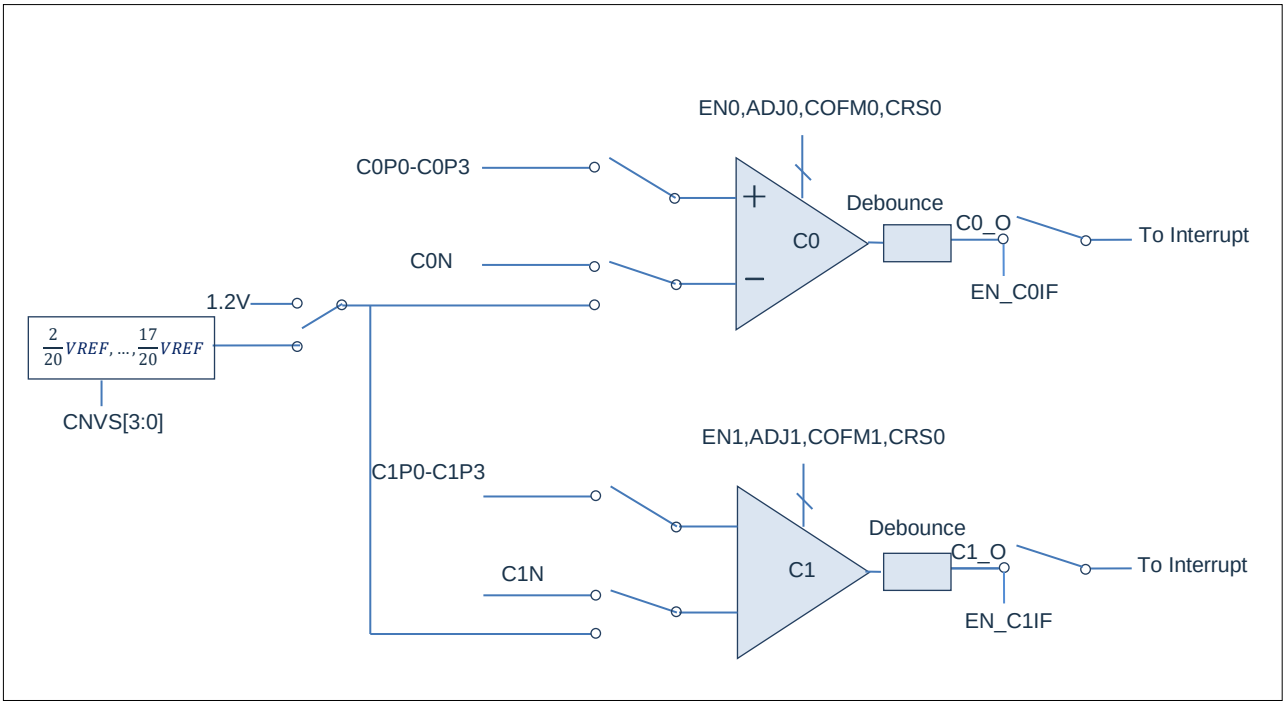


Figure 3-12: Block diagram of Comparator

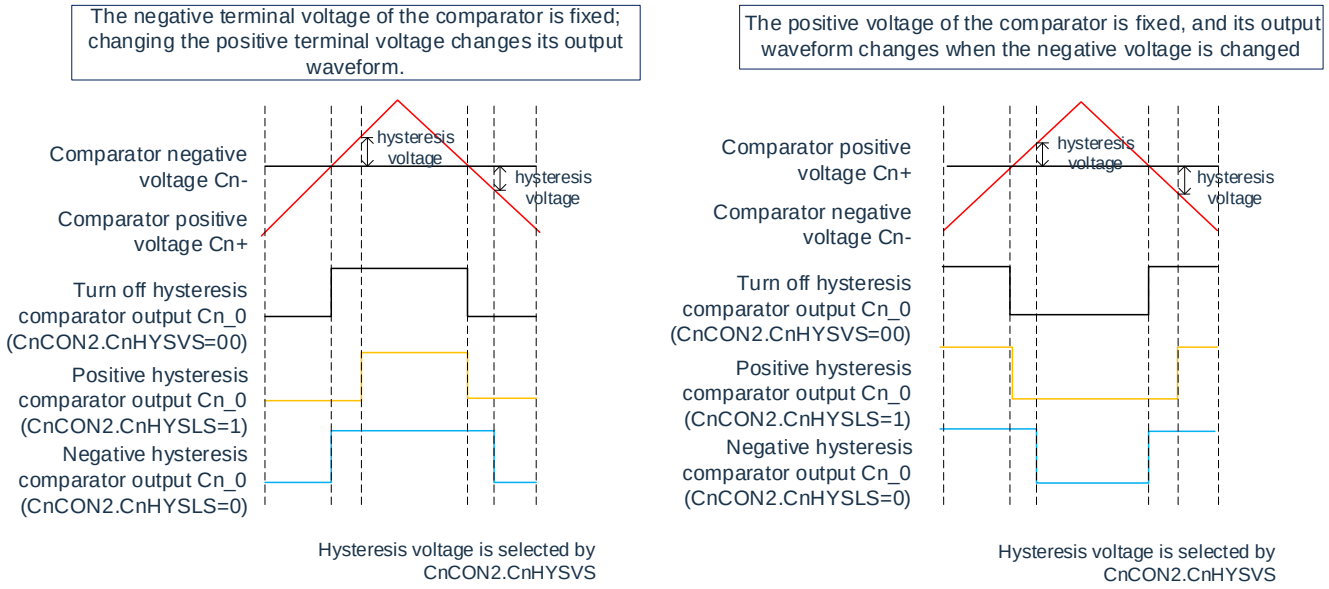


Figure 3-13: Block diagram of comparator hysteresis function

3.14.4 Register mapping

(ACMP base address = 0x4D00_0000)

RO: read only, WO: write only, R/W: both read and write

Register	Offset value	R/W	Description	Reset value
C0CON0(P1B)	0x000	R/W	Analog comparator 0 control register 0	0x0
C0CON1(P1B)	0x004	R/W	Analog comparator 0 control register 1	0x10
C0CON2(P1B)	0x008	R/W	Analog comparator 0 control register 2	0x0
C0ADJE(P1B)	0x00C	R/W	Analog comparator 0 adjust enable register	0x0
C1CON0(P1B)	0x010	R/W	Analog comparator 1 control register 0	0x0
C1CON1(P1B)	0x014	R/W	Analog comparator 1 control register 1	0x10
C1CON2(P1B)	0x018	R/W	Analog comparator 1 control register 2	0x0
C1ADJE(P1B)	0x01C	R/W	Analog comparator 1 adjust enable register	0x0
CVRCON(P1B)	0x020	R/W	Analog comparator reference voltage control register	0x0
CVECON(P1B)	0x024	R/W	Analog comparator event control register	0x0
IMSC(P1B)	0x028	R/W	Analog comparator interrupt enable register	0x0
RIS	0x02C	RO	Analog comparator interrupt source status register	0x0
MIS	0x030	RO	Analog comparator enabled interrupt status register	0x0
ICLR	0x034	WO	Analog comparator interrupt clear register	0x0
LOCK	0x038	R/W	Analog comparator write enable register	0x0

Note: The registers marked (P1B) are protected registers.
(P1B): When LOCK=55H, the labeled register is allowed to write; = Other values, forbidden to write.

3.14.5 Register description

3.14.5.1 Analog comparator n control register 0(CnCON0)(n=0-1)

Bit	Symbol	Description	Reset value
31:16	-	Reserved	-
15	CnEN	Analog comparator n enable bit 0: Disable 1: Enable	0x0
14	CnCOFM	Analog comparator n adjustment mode enable bit 0: Disable 1: Enable	0x0
13	CnN2GND	Analog comparator n adjustment mode negative ground enable bit 0: Disable 1: Enable	0x0
12:8	-	Reserved	-
7:4	CnPS	Analog comparator n positive channel selection bit 000: CnP0 001: CnP1 010: CnP2 011: CnP3 1xx: Prohibit selection	0x0
3:0	CnNS	Analog comparator n negative channel selection bit 00: CnN 01: Vref (Bandgap or k×VDD) 1x: Disable	0x0

3.14.5.2 Analog comparator n control register 1(CnCON1)(n=0-1)

Bit	Symbol	Description	Reset value
31:10	-	Reserved	-
9	CnOUT	Analog comparator n result bit (Read-only)	0x0
8	CnCRS	Analog comparator n adjust mode input select bit 0: Negative 1: Positive	0x0
7:5	-	Reserved	-
4:0	CnADJ	Analog comparator n adjustment bit	0x10

3.14.5.3 Analog comparator n control register 2(CnCON2)(n=0-1)

Bit	Symbol	Description	Reset value
31:13	-	Reserved	-
12	CnHYSLS	Analog comparator n hysteresis mode control bit (single hysteresis function is supported only) 0: Positive hysteresis 1: Negative hysteresis See the corresponding block diagram in the function description	0x0
11:10	CnHYSVS	Analog comparator n hysteresis voltage selection (invalid in adjust mode). 00: No hysteresis 01: 10mV 10: 20mV 11: 60mV	0x0
9	CnPOS	Analog comparator n output polarity select bit 0: Normal output 1: Reverse output	0x0
8	CnFE	Analog comparator n output filtering enable bit 0: Disable 1: Enable	0x0
7:4	-	Reserved	-
3:0	CnFS	Analog comparator n output filtering time selection bit 0000: (0~1)×Tpclk 0001: (1~2)×Tpclk 0010: (2~3)×Tpclk 0011: (4~5)×Tpclk 0100: (8~9)×Tpclk 0101: (16~17)×Tpclk 0110: (32~33)×Tpclk 0111: (64~65)×Tpclk 1000: (128~129)×Tpclk 1001: (256~257)×Tpclk 1010: (512~513)×Tpclk Other: (0~1)×Tpclk	0x0

3.14.5.4 Analog comparator n adjust enable register (CnADJE)(n=0-1)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	CnADJE	AAH: This is determined by the OPnADJ < 4:0 > in the CnCON1 register Other: Determined by the CONFIG relevant bit	0x0

3.14.5.5 Analog comparator reference voltage control register (CVRCON)

Bit	Symbol	Description	Reset value
31:6	-	Reserved	-
5:4	CSVR	Analog comparator negative reference voltage selection bit 0x: Select 1.2V (Bandgap) 10: Select k×VDD 11: Select k×1.2V (0.12V~1.02V)	0x0
3:0	CVS	Analog comparator reference voltage divider k select bit 0000: 2/20 0001: 3/20 …… …… 1111: 17/20 Note: - Step for selecting VDD divider voltage is VDD(1/20). - Step for selecting 1.2V divider voltage is 60mV.	0x0

3.14.5.6 Analog comparator event control register (CEVCON)

Bit	Symbol	Description	Reset value
31:6	-	Reserved	-
5	EVE1	Analog comparator 1 event output enable bit (does not affect interrupt generation) 0: Disable 1: Enable	0x0
4	EVE0	Analog comparator 0 event output enable bit (does not affect interrupt generation). 0: Disable 1: Enable	0x0
3:2	EVS1	Analog comparator 1 event generation condition select bit 00: Comparator 1 outputs a transition from 0->1 01: Comparator 1 outputs a transition from 1->0 10: Comparator 1 outputs a transition from 0->1 or a transition from 1->0 11: Reserved	0x0
1:0	EVS0	Analog comparator 0 event generation condition selection bit 00: Comparator 0 outputs a transition from 0->1 01: Comparator 0 outputs a transition from 1->0 10: Comparator 0 outputs a transition from 0->1 or a transition from 1->0 11: Reserved	0x0

3.14.5.7 Analog comparator interrupt enable register (IMSC)

Bit	Symbol	Description	Reset value
31:2	-	Reserved	-
1	EN_C1IF	Analog comparator 1 interrupt enable bit 0: Disable 1: Enable	0x0
0	EN_C0IF	Analog comparator 0 interrupt enable bit 0: Disable 1: Enable	0x0

3.14.5.8 Analog comparator interrupt source status register (RIS)

Bit	Symbol	Description	Reset value
31:2	-	Reserved	-
1	RIS_C1IF	Analog comparator 1 interrupt source status bit 0: No interruptions generated 1: An interrupt is generated (event generation)	0x0
0	RIS_C0IF	Analog comparator 0 interrupt source status bit 0: No interruptions generated 1: An interrupt is generated (event generation)	0x0

3.14.5.9 Analog comparator enabled interrupt source status register (MIS)

Bit	Symbol	Description	Reset value
31:2	-	Reserved	-
1	MIS_C1IF	Analog comparator 1 enabled interrupt status bit 0: No interruptions generated 1: An interrupt is generated	0x0
0	MIS_C0IF	Analog comparator 0 enabled interrupt status bit 0: No interruptions generated 1: An interrupt is generated	0x0

3.14.5.10 Analog comparator interrupt clear control register (ICLR)

Bit	Symbol	Description	Reset value
31:2	-	Reserved	-
1	ICLR_C1IF	Analog comparator 1 interrupt clear control bit 0: Does not affect 1: Clear the RIS_C1IF flag bit	0x0
0	ICLR_C0IF	Analog comparator 0 interrupt clear control bit 0: Does not affect 1: Clear the RIS_C0IF flag bit	0x0

3.14.5.11 Analog comparator write enable control register (LOCK)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	LOCK	When LOCK=0x55, enable the operation of ACMP related registers. (See ACMP register mapping for details.) When LOCK=other values, disable the operation of ACMP related registers.	0x0

3.15 Memory control module (FMC)

3.15.1 Overview

This is a 32KB on-chip FLASH, used to store the application program. A user configuration area for system initialization. It supports In Application Programming (IAP), which performs a switch between the bootloader and user program without an external reset after updating the FLASH program.

3.15.2 Features

- Support 32KB application program memory (APROM).
- Support BOOT function, BOOT area and APROM share 32KB space, size can be set 1KB/2KB/4KB.
- Support 1KB data storage area, does not occupy 32KB program space.
- Support 512-byte page erase for all on-chip FLASH operations.
- Support In-System Programming (ISP)/In-Application Programming (IAP) to update the on-chip Flash.
- Support CRC calculation and detection for program space code of arbitrary interval.

3.15.3 Feature description

3.15.3.1 Memory structure

The on-chip FLASH contains 32KB user program area (APROM), 512 Byte user configuration area.

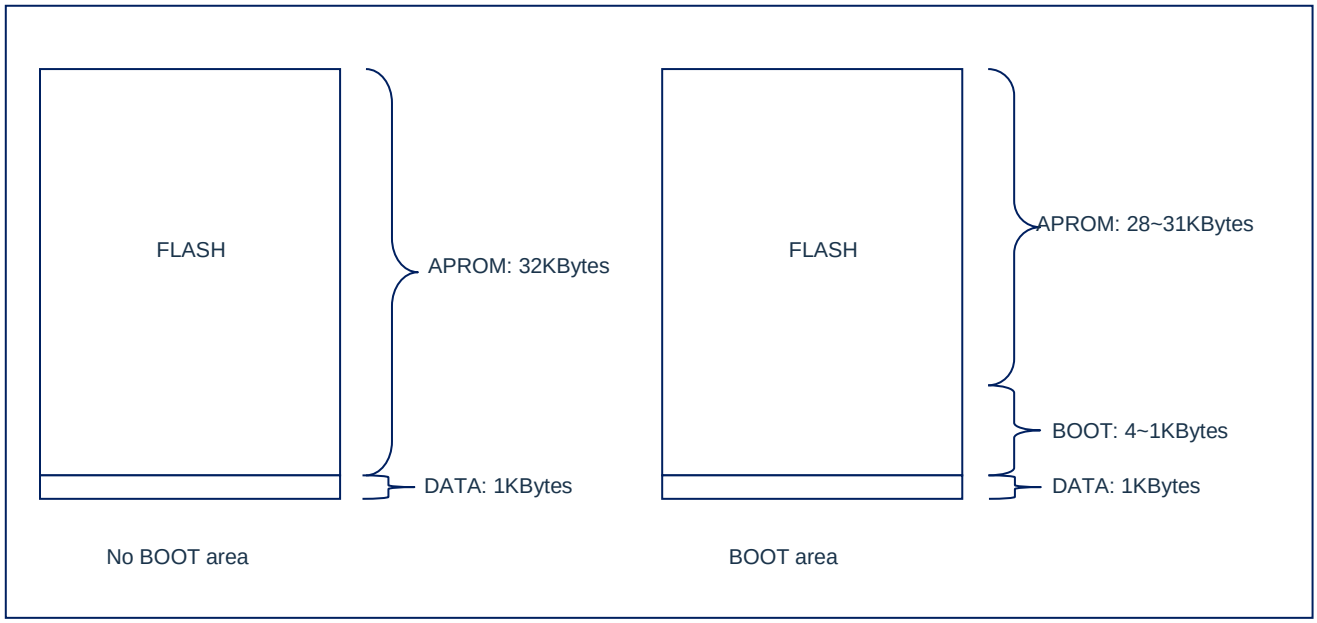


Figure 3-14: Storage structure diagram

3.15.3.2 Flash operation

Erase: Includes two commands: overall erase and page erase.

1) The 32KB of APROM space is erased when the whole program is erased. The overall erase operation is as follows.

- Enable access to FMC related registers.
- Wait for FMC to become idle.
- Write 0x06 in FMCCMD.
- Waiting for FMC to be idle.
- Disable access to FMC related registers.

2) During page erase, 0x200 address space can be erased per page. The page erase operation method is as follows.

- Enables access to FMC related registers.
- Write page erase first address in FMCADR.
- Wait for FMC to become idle.
- Write 0x03 in FMCCMD.
- Wait for FMC to become idle.
- Disable access to FMC related registers.

Programming: After the erase is completed, the page data can be programmed continuously. The programming is as follows:

1) Enable access to FMC related registers.
2) Set the address to be programmed in FMCADR.
3) Write the data to be programmed in FMCDAT.
4) Wait for FMC to become idle.
5) Write 0x02 in FMCCMD.
6) Wait for FMC to become idle.
7) Disable access to FMC related registers.

Reading: Two types of reading are included.

1) Direct addressing mode, read 0x0000-0x7FFF address directly.
2) Read by FMC command, the operation sequence is as follows.

- Enable access to FMC related registers.
- Set the address to be read in FMCADR.
- Write 0x01 in FMCCMD.
- Read the FMCDAT value.
- Disable access to FMC related registers.

3.15.3.3 Flash space CRC checksum

See the <Security Related> section for details.

3.15.3.4 Flash space program start selection

The chip can be configured to boot from APROM or from the BOOT area after power-on reset. The relevant choices are selected in the User Configuration area:

BOOT_TYPE	Power-on Boot selection instruction
1111	Boot from APROM
0001	Boot from BOOT area
0000	Boot from BOOT area, requires BOOT pin to be grounded.
Other	Boot from APROM

If you need to start from BOOT, you need to allocate valid space to BOOT area: 1Kbytes/ 2Kbytes/ 4Kbytes.

If the space allocated for BOOT is 0Kbytes, even if BOOT_TYPE selects to start from BOOT area, it actually boots from APROM.

After selecting to start the boot program from the BOOT area, it is recommended to perform the following steps if you need to go to the APROM program execution:

1) Write 1 to the ISPS bit of the FMCCON register to allow the next reset program to be executed from the APROM.
2) Write 0x55AA669A to the RSTCON register to allow a system reset (does not reload the boot configuration).
3) After a system reset, the program will be executed from the APROM area.

After the program is run in APROM, if it is necessary to go to the BOOT area for execution, it is recommended to perform the following steps:

1) Write the ISPS bit of the FMCCON register to 0, allowing the next reset procedure to be executed from the BOOT area.
2) Write the RSTCON register to 0x55AA669A, allowing the system to reset (without reloading the boot configuration).
3) After the system resets, the program will be executed from the BOOT area.

3.15.4 Register mapping

(FMC base address = 0x4980_0000)

RO: read only; WO: write only; R/W: read and write.

Register	Offset value	R/W	Description	Reset value
CON(P1D)	0x000	R/W	FMC control register	-
ADR(P1D)	0x004	R/W	FMC address register (FMC CRC check start address register)	0x0
DAT(P1D)	0x008	R/W	FMC data register	0x0
CMD(P1D)	0x00C	R/W	FMC command register	0x0
LOCK	0x010	R/W	FMC access enable register	0x0
CRCEA(P1D)	0x020	R/W	FMC CRC end address register	0Xffff
CRCIN(P1D)	0x024	R/W	FMC CRC input register	0x0
CRCD(P1D)	0x028	R/W	FMC CRC data register	0x0

Note: The registers marked (P1D) are protected registers.

(P1D): When LOCK=55AA6699H, the marked register is allowed to write; = Other values, forbidden to write.

3.15.5 Register description

3.15.5.1 FMC control register (CON)

Bit	Symbol	Description	Reset value
31:6	-	Reserved	-
5	BUSY	FMC busy 0: FMC idle 1: FMC is busy, erasing, programming or reading operations are performed normally.	0x0
4	ISPS	Select the location where the program starts after the next reset (Excluding power-on reset, MCURST reset, external reset). 0: After the reset, the program is executed from BOOT (BOOT region and BOOT enable need to be configured). 1: After the reset, the procedure is performed from the APROM	0x1
3:0	-	Reserved	-

3.15.5.2 FMC address register (ADR)

Bit	Symbol	Description	Reset value
31:0	ADDR	Word operation address (or start address of CRC operation) 0x00xx_xxxx (APROM) 0x1cxx_xxxx (DATA area) (The lower two bits must be 00)	0x0

3.15.5.3 FMC data register (DAT)

Bit	Symbol	Description	Reset value
31:0	FMCDAT	When a write operation is performed, the data is written to FLASH, and when a read operation is performed, the FLASH data is returned	0x0

3.15.5.4 FMC command register (CMD)

Bit	Symbol	Description	Reset value
31:5	-	Reserved	-
4:0	FMCFUNC	FMC function 0x0: Reserved 0x1: Read data 0x2: Write data (50us). 0x3: Page erase (4.7ms).	0x0

		0Xd: CRC check (CRC16-CCITT) Other: Reserved	

3.15.5.5 FMC access enable register (LOCK)

Bit	Symbol	Description	Reset value
31:0	FMCLOCK	Write 0x55AA6699 to enable operation of other FMC registers, the read value is 1. Write 0x55AA6699, enable operation of other FMC registers, read the value as 0.	0x0

3.15.5.6 FMC CRC check end address register (CRCEA)

Bit	Symbol	Description	Reset value
31:16	-	Reserved	-
15:0	CRCEA	CRC check end address	0x0

3.15.5.7 FMC CRC input register (CRCIN)

Bit	Symbol	Description	Reset value
31:8	-	Reserved	-
7:0	CRCIN	CRC input 8-bit data to be calculated	0x0

3.15.5.8 FMC CRC data register (CRCD)

Bit	Symbol	Description	Reset value
31:16	-	Reserved	-
15:0	CRCD	CRC saves the 16-bit result of the operation.	0x0

3.16 Security related

3.16.1 Overview

The chip supports functions related to code security and application security.

3.16.2 Unique chip identification number (UID)

Each chip has a different 96-bit unique identification number, or unique identification. It has been set at the factory and cannot be modified by the user. The chip UID is read through the memory module when used. (This feature requires support from the relevant CMS department).

There are two ways to read UIDs:

1) Read by the FMC module, the corresponding address mapping is as follows:

(Memory base address= 0x1800_0000) RO: read only; WO: write only; R/W: read and write.

Address	Offset value	R/W	Description	Reset value
Reserved	0x000	-	Reserved	-
UID0	0x004	RO	UID[31:0]	-
UID1	0x008	RO	UID[63:32]	-
UID2	0x00C	RO	UID[95:64]	-

2) Read by the system control module SYSCON, the corresponding address mapping is as follows:

(Register base address= 0x5000_0000) RO: read only; WO: write only; R/W: read and write.

Address	Offset value	R/W	Description	Reset value
Reserved	0x000	-	Reserved	-
CIDL	0x034	RO	UID[63:32]	-
CIDH	0x038	RO	UID[95:64]	-
UIDX	0x500	RO	UID[31:0]	-

3.16.3 User unique chip identification number (USRUID)

The chip has an additional 128-bit chip ID, USRUID, which consists of a 96-bit user configurable ID and a 32-bit fixed ID, which differs from the UID in that the USRUID is not readable by the program. The user can set the unique 96-bit identification number in the CMS tool. The other 32 bits are not operable.

The 128-bit USRUID can be used as a key in encrypted applications, which can be detected by the user program to establish a protection mechanism.

Program to prevent the decryption operation mechanism: if the detection result is incorrect, then immediately disable the USRUID detection, and the detection operation will be ignored, it needs to be reset to be able to detect again, the single detection fault tolerance rate is 0.

USRUID in the User Configuration has a separate encryption bit, set the USRUID to encrypted state, any other methods and tools can not read out the data.

Tests are carried out in the following ways.

There are four registers in the system control module, UUIDWC0, UUIDWC1, UUIDWC2, UUIDWCS, which are used to detect the USRUID data. If all the data written to UUIDWC0-UUIDWC2 (write 96bit user ID), UUIDWCS (must write 0Xffffffff) are the same as the preset USRUID data, then the values of these registers are read as 0x1, otherwise it is 0.

Mechanism to prevent decryption operation in the program: If the data written is incorrect, the USRUID detection operation is immediately disabled, and the operation of writing to the USRUID again will be ignored, and it needs to be reset to detect again, and the single detection tolerance rate is 0.

3.16.4 Protection of program code

The chip supports the protection function of the chip code and the code partition protection function.

APROM partition protection: The 32KBytes space is divided into 16 segments, each with a size of 2KBytes, and the protection state can be set separately in the user configuration register CFG_APROMPE. If a BOOT interval has been assigned, the protection state acts within the valid area.

APROM protection status description												
Bit	Address	Valid status	Read			Programming			Erase			Default value
			NM	SW	BT	NM	SW	BT	NM	SW	BT	-
0	0x0000-0x07FF	0	✓	×	✓	×	×	✓	×	×	✓	1
1	0x0800-0x0FFF	0	✓	×	✓	×	×	✓	×	×	✓	1
2	0x1000-0x17FF	0	✓	×	✓	×	×	✓	×	×	✓	1
3	0x1800-0x1FFF	0	✓	×	✓	×	×	✓	×	×	✓	1
4	0x2000-0x27FF	0	✓	×	✓	×	×	✓	×	×	✓	1
5	0x2800-0x2FFF	0	✓	×	✓	×	×	✓	×	×	✓	1
6	0x3000-0x37FF	0	✓	×	✓	×	×	✓	×	×	✓	1
7	0x3800-0x3FFF	0	✓	×	✓	×	×	✓	×	×	✓	1
8	0x4000-0x47FF	0	✓	×	✓	×	×	✓	×	×	✓	1
9	0x4800-0x4FFF	0	✓	×	✓	×	×	✓	×	×	✓	1
10	0x5000-0x57FF	0	✓	×	✓	×	×	✓	×	×	✓	1
11	0x5800-0x5FFF	0	✓	×	✓	×	×	✓	×	×	✓	1
12	0x6000-0x67FF	0	✓	×	✓	×	×	✓	×	×	✓	1
13	0x6800-0x6FFF	0	✓	×	✓	×	×	✓	×	×	✓	1
14	0x7000-0x77FF	0	✓	×	✓	×	×	✓	×	×	✓	1
15	0x7800-0x7FFF	0	✓	×	✓	×	×	✓	×	×	✓	1

NM = Normal

SW = SWD status

BOOT = BOOT status

BOOT partition protection: The 4KBytes space is divided into 4 segments, each segment is 1KBytes, and the protection status can be set separately in the user configuration register CFG_BOOTPE. If an APROM interval has been assigned, the protection state acts within the valid BOOT region.

BOOT area protection status description												
Bit	Address	Valid status	Read			Programming			Erase			Default value
			NM	SW	BT	NM	SW	BT	NM	SW	BT	-
0	0x7000-0x73FF	0	×	×	×	×	×	×	×	×	×	1
1	0x7400-0x77FF	0	×	×	×	×	×	×	×	×	×	1
2	0x7800-0x7BFF	0	×	×	×	×	×	×	×	×	×	1
3	0x7C00-0x7FFF	0	×	×	×	×	×	×	×	×	×	1

NM = Normal

SW = SWD status

BOOT = BOOT status

3.16.5 Program CRC checksum

3.16.5.1 CRC calculation for Flash space

The chip supports the hardware calculation program CRC. The FMC control module supports hardware to automatically calculate the value of CRC16. The check interval can be set arbitrarily. The CRC is generated using the polynomial CRC-16-CCITT "$X^{16}+X^{12}+X^5+1$", The relevant registers are as follows:

FMCADR:	Start address register for the CRC checksum
FMCCRCEA:	End address register for the CRC checksum (FMCRCCEA>=FMCADR is required)
FMCCRCIN:	Input register for the CRC checksum
FMCCRCD:	Data register for the CRC checksum (holds 16-bit results of CRC checksum)

The steps to calculate the CRC are as follows:

1) Set the starting address of the required check space in FMCADR
2) Set the end address of the required check space in FMCCRCEA, which must be greater than or equal to FMCADR
3) Write FMCCRCIN to 0x00
4) Write FMCCRCD to 0x0000, clear the previous results
5) Write FMCCMD to 0xD and start the CRC checksum
6) After the CRC checksum is completed, the BUSY bit in FMCCON will be set to 0
7) Read the FMCCRCD data, that is, the calculated CRC

The CPU stops during the flash space checking process and continues to run after the calculation is completed. The CRC check is done in byte mode (8-bit), from the initial address to the end address.

For example, if the data of address 0x0 is 12H, the data of address 0x1 is 34H, the data of address 0x2 is 56H, and the data of address 0x3 is 78H, then the CRC value will be calculated according to the order of 12H->34H->56H->78H, and the final checksum will be 67F0H.

Checksum of 32Kbytes program space takes about 1ms@Fsys=48MHz.

The CRC check of the Flash space is valid for the absolute address of the Flash, and is not affected by the protection state or BOOT state.

3.16.5.2 Flash space CRC checksum comparison

The program CRC checksum is recommended to be generated using the polynomial CRC-16-CCITT of "$X^{16}+X^{12}+X^5+1$". This uses the same polynomial in FMC as the CRC module to quickly verify that the program code is correct. (CMS-related tool support is required when using this function).

There are two ways to read PCRCD:

1) Read by the FMC module, the corresponding address mapping is as follows:

(Memory address = 0x1000_0000) RO: read only; WO: write only; R/W: read and write.

Address	Offset value	R/W	Description	Reset value
PCRCD	0x01C	RO	PCRCD	-

2) Read by the system control module SYSCON, the corresponding address mapping is as follows:

(Register base address= 0x5000_0000) RO: read only; WO: write only; R/W: read and write.

Address	Offset value	R/W	Description	Reset value
PCRCD	0x510	RO	{ 16'h0, PCRCD }	-

3.16.6 CRC operation (general CRC)

The universal CRC module verifies the correctness of the program or data transmission. The CRC operations of the general-purpose module operate at the APB clock.

The polynomial of CRC is "$X^{16}+X^{12}+X^5+1$" of CRC-16-CCITT.

3.16.7 Memory illegal access detection

Access to the illegal memory address in the ARM microcontroller generates an error exception, which provides a better method of detecting program errors and allows software errors to be detected earlier.

In an AHB system connected to a Cortex-M0 processor, the address resolution logic probes for the address being accessed, and if an illegal location is being accessed, the bus system responds with an error signal that can cause a bus error by taking values or data access.

3.16.8 SRAM protection function

The on-chip SRAM is write-protected and can be set to zone write-protected. Write protection does not affect the read function, the system register SRAMLOCK can set the relevant function.

3.16.8.1 SRAM write enable register (SRAMLOCK)

Bit	Symbol	Description	Reset value
31:16	LOCK	When LOCK=0x55AA, SRAM write-protect function is effective.	0x0
15:4	-	Reserved	-
3:0	REGION	Bit3: Set SRAM address 0x20001800-0x20001FFF area to write-protect state Bit2: Set SRAM address 0x20001000-0x200017FF area to write-protected state Bit1: Set SRAM address 0x20000800-0x20000FFF area to write-protected state Bit0: -- Write 0 protection disabled (read/write) Write 1 protection enabled (read only) Note: The 2Kbytes area of the SRAM initial address range of 0x20000000-0x200007FF is free for reading and writing.	0x0

3.16.9 SFR guard function

Some SFRs of the key function modules have guard functions and can be set to level protection. The associated registers with SFR guard can be referred to the register mapping instructions for each module.

The protection level types are as follows:

Level	Type	Description
0	P0	When data is written, other data is detected at the same time (A569H/55AAH)
1	P1A	When data is written, other register values are detected (55H/AAH/99H)
2	P1B	When data is written, other register values are detected (55H)
3	P1C	When data is written, other register values are detected (55AAH)
4	P1D	When data is written, other register values are detected (55AA6699H).
5	P2	Reserved

For example, GPIO, IOCFG, WDT, FMC, CCP0/1, EPWM, ACMP0/1, ADC1 and other function modules have similar protection lock registers to realize SFR guard function. For specific use, please refer to the instruction of each module.

3.16.10 ADC test function

This A/D test function verifies that the A/D converter is operating properly by converting the A/D converter' s positive reference voltage, negative reference voltage, analog input channel (ANi), and internal reference voltage.

The ADC1 supports the test functions of the ADC.

3.16.11 GPIO pin voltage level detection

When the port is configured as a GPIO as the output port, the status of the pin can also be read. That is, it can detect the IO port as the output port, and can also detect whether the preset level value of the output is correct. In GPIO function mode, whether the port is configured as an output port or an input port, the pin level can be read via GPIO->DI.

Each set of GPIO input circuits supports filtering and is selectable in filter width. The GPIOxDIDB register determines whether to filter and the sample clock for filtering. The basic sample clock of the filter is HCLK, and a total of 8 sample clocks can be selected from HCLK-HCLK/14.

After three consecutive samples by the sample clock, if they are all at the same level, the pin level is considered stable. If it is not the same, the pin level is considered to be jittery, and the read value is the state of the level before jitter. The structure filters out glitches less than 2× Ts (sample clock cycle) widths.

4. Electrical Characteristics

4.1 Absolute maximum rating

Symbol	Parameter	Min.	Max.	Unit
V_{DD}-V_{SS}	Supply voltage	-0.3	5.8	V
V_{IN}	Input voltage	VSS-0.3	VDD+0.3	V
T_A	Operating temperature	-40	+105	℃
T_{ST}	Storage temperature	-55	+150	℃
I_{DD}	V_{DD} maximum input current	-	120	mA
I_{SS}	V_{SS} maximum output current	-	120	mA
I_{IO}	Single IO maximum sink current	-	50	mA
	Single IO maximum output current	-	40	mA
	All IO maximum sink current	-	100	mA
	All IO maximum output current	-	100	mA

4.2 D.C. electrical characteristic

(V_{DD}-V_{SS}=2.1~5.5V, T_A=25°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	HCLK=64MHz	2.1	-	5.5	V
I_{DD1}	Operating current	HCLK=64MHz,HSI=64MHz, ALL APBCLK OFF,V_{DD}=5.0V	-	12	-	mA
I_{DD2}		HCLK=64MHz,HSI=64MHz, ALL APBCLK OFF,V_{DD}=3.3V	-	12	-	mA
I_{DD3}		HCLK=48MHz,HSI=48MHz, ALL APBCLK OFF,V_{DD}=5.0V	-	9	-	mA
I_{DD4}		HCLK=48MHz,HSI=48MHz, ALL APBCLK OFF,V_{DD}=3.3V	-	9	-	mA
I_{DD5}		HCLK=40KHz,LSI=40KHz, ALL APBCLK OFF,V_{DD}=5V	-	2.5	-	mA
I_{DD6}		HCLK=40KHz,LSI=40KHz, ALL APBCLK OFF,V_{DD}=3.3V	-	2.5	-	mA
V_{IL}	Input low level	-	VSS	-	0.3VDD	V
V_{IH}	Input high level	-	0.7VDD	-	VDD	V
I_{OL1}	Low-level output current	V_{DD}=5V GPIOxDR[n]=0 VIO=1.5V	-	-	50	mA
I_{OL2}	Low-level output current	V_{DD}=5V GPIOxDR[n]=1 VIO=1.5V	-	-	25	mA
I_{OH1}	High-level output current	V_{DD}=5V GPIOxDR[n]=0 VIO=3.5V	-	-	40	mA
I_{OH2}	High-level output current	V_{DD}=5V GPIOxDR[n]=1 VIO=3.5V	-	-	20	mA
R_{UP}	Pull-up resistor	-	-	33	-	KΩ
R_D	Pull-down resistor	T_A=25°C, VDD=5V, V_{IO}=0.3VDD	-	33	-	KΩ
F_{AHBCLK}	AHB clock	-	-	-	64	MHz
F_{APBCLK}	APB clock	-	-	-	64	MHz

4.3 A.C. electrical characteristic

4.3.1 Power-on reset time

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{RESET}	Reset time	VDD=5V	-	4.5	-	ms
T_{VDDR}	VDD rise rate	VDD=5V	2	-	∞	us/V
T_{VDDF}	VDD fall rate	VDD=5V	2	-	∞	us/V

4.3.2 Internal high-speed oscillator (HSI)

Symbol	Parameter	Condition	Min.	Typ.	Max.
V_{HSI}	Operating voltage	2.1	-	5.5	V
T_A	Operating temperature	-40	-	105	℃
I_{HSI}	Operating current V_{DD}=5.0V,T_A=25℃	-	300	-	uA
F_{HSI}	T_A=25℃,V_{DD}=5.0V	-	64	-	MHz
	T_A=25℃,V_{DD}=2.1~5.5V	-0.5	-	+0.5	%
	T_A=-40℃~105℃,V_{DD}=2.1~5.5V	-2.5	-	+1.0	%

4.3.3 Internal 40KHz low-speed oscillator (LSI)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{LSI}	Operating voltage	2.1	-	5.5	V
T_A	Operating temperature	-40	-	105	℃
I_{LSI}	Operating current V_{DD}=5.0V,T_A=25℃	-	10	-	uA
F_{LSI}	T_A=25℃,V_{DD}=5.0V	-	40	-	KHz
	T_A=25℃,V_{DD}=2.1~5.5V	-5.0	-	+5.0	%
	T_A=-40℃~105℃,V_{DD}=2.1~5.5V	-50	-	+50	%

4.3.4 Low voltage reset electrical parameter

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{LVR1}	Low-voltage detection threshold 1.9V	1.75	1.9	2.05	V
V_{LVR2}	Low-voltage detection threshold 2.1V	1.95	2.1	2.25	V
V_{LVR3}	Low-voltage detection threshold 2.6V	2.45	2.6	2.75	V

4.4 BANDGAP electrical characteristic

VDD=2.1V-5.5V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Bit
V_{REF}	Internal reference 1.2V	T_A=-40℃ to 105℃	1.188	1.2	1.212	V

4.5 ADC1 electrical characteristic

Symbol	Parameter	Min	Typ.	Max.	bit
V_{AVDD}	ADC operating voltage	2.5	-	5.5	V
V_{AIN}	Analog signal input	0	-	V_{AVDD}	V
N_R	Resolution	12			Bit
T_{ADCK}	ADC clock cycle	0.0325	-	5.3	us
T_{ADC}	AD conversion time (Sample hold time: 10.5×T_{ADC})	-	23	-	T_{ADCK}
F_C	Conversion rate	1.4			Msps
F_S	Sampling rate	1.2			Msps

4.6 FLASH electrical parameter

Symbol	Parameter	Condition	Min.	Typ.	Max.	Bit
V_F	Flash operating voltage	-	2.1	-	5.5	V
T_F	Flash operating temperature	-	-40	27	125	℃
$N_{ENDURANCE}$	Endurance	-	20,000	-	-	Cycle
T_{RET}	Data retention	25℃	100	-	-	year
T_{ERASE}	Sector erase time	-	-	4.7	-	ms
T_{WRITE}	Byte write time	-	-	50	-	us
I_{DD1}	Read current	-	-	-	3.5	mA
I_{DD2}	Program current	-	-	-	3.5	mA
I_{DD3}	Erase current	-	-	-	2	mA
I_{DD4}	Standby current	25℃-125℃	-	-	7	uA

4.7 OP electrical parameter

T_A=25℃, V_{SENSE}=V_{IN+}-V_{IN-}, VDD=5V, V_{IN+}=1V, unless otherwise indicated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply voltage	-	2.5	-	5.5	V
I_Q	Static current	V_{SENSE}=0mV	-	0.8	1.3	mA
I_{SD}	Shutdown current	-	-	5	-	nA
T_A	Operating temperature	-	-40	25	105	℃
Input characteristic						
V_{OS}	Input offset voltage	No trimming	-	±3.8	-	mV
		After trimming	-	±0.5	-	
V_{CM}	Common-mode input range	-40℃~105℃	0	-	VDD-1.5	V
I_B	Input bias current	V_{SENSE}=0mV	-	10	-	pA
I_{OS}	Input offset current	V_{SENSE}=0mV	-	10	-	pA
Output characteristic						
C_{LOAD}	Capacitive load	-	-	30	-	pF
V_{OH}	Maximum output voltage	-40℃~105℃	-	-	VDD-0.3	V
V_{OL}	Minimum output voltage	-40℃~105℃	0.3	-	-	V
Frequency characteristic						
A_{OL}	Open loop gain	-	-	105	-	dB
BW	Bandwidth	C_{LOAD}=30pF	-	5	-	MHz
PSRR	Power supply rejection ratio	VDD=2.5~5.5V, V_{IN+}=1V, V_{SENSE}=0mV	-	59	-	dB
CMRR	Common mode rejection ratio	V_{IN+}=0.3~ (VDD-1.5) -40℃~105℃	-	110	-	dB
Transient characteristic						
SR	Slew rate	C_{LOAD} =30pF	-	±5	-	V/μs
		R_{LOAD}=2K,C_{LOAD}=100pF	-	±4	-	V/μs
T_{STB}	Stable time	-	-	-	1.5	μs

4.8 PGA electrical parameter

T_A=25℃, VDD=5V, V_{IN+}=0.1V, take 10 times gain (Av) as an example, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply voltage	-	2.5	-	5.5	V
I_Q	Static current	V_{OUT}=2V	-	0.9	1.6	mA
I_{SD}	Shutdown current	-	-	10	-	nA
T_A	Operating temperature	-	-40	25	105	℃
Input characteristic						
V_{OS}	Input offset voltage	-	-	±3.0	-	mV
V_{CM}	Common mode input voltage range	-40℃~105℃	0.35/G	-	(VDD-0.35)/ G	V
I_B	Input bias current	-	-	10	-	pA
I_{OS}	Input offset current	-	-	10	-	pA
Output characteristic						
EG	Gain error	G=4,8	-1	-	1	%
		G=10,12,14,16	-1.5	-	1.5	
		G=32	-2	-	2	
C_{LOAD}	Capacitive load	-	-	10	-	pF
V_{OH}	Maximum output voltage (internal)	-40℃~105℃	-	VDD-0.3	-	V
V_{OL}	Minimum output voltage	-40℃~105℃	-	0.3	-	V
V_{A0O} V_{A1O}	Test output port of PGA0/1	-40℃~105℃	-	-	3.7	V
Frequency characteristic						
BW	Bandwidth	R_{LOAD}=0.8MΩ, C_{LOAD}=3pF,G=4	-	2	-	MHz
PSRR	Power rejection ratio	VDD=2.5~5.5V	-	75	-	dB
CMRR	Common mode rejection ratio	-40℃~105℃	-	80	-	dB
Transient characteristic						
SR	Slew rate	R_{LOAD}=0.8MΩ, C_{LOAD}=3pF	-	6	-	V/μs
		R_{LOAD}=2KΩ, C_{LOAD}=100pF	-	4	-	V/μs
T_{STB}	Stable time	-	-	-	2	μs

4.9 ACMP electrical parameter

T_A=25℃, V_{SENSE}=V_{IN+}-V_{IN-}, VDD=5V, V_{IN+}=1V, unless otherwise indicated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply voltage	-	2.1	-	5.5	V
I_Q	Static current	V_{SENSE}=0.1V	-	0.3	0.4	mA
I_{SD}	Shutdown current	V_{SENSE}=0.1V	-	5	-	nA
T_A	Operating temperature	-	-40	25	105	℃
Input characteristic						
V_{OS}	Input offset voltage Common mode input voltage range	No trimming	-	±4.0	-	mV
		After trimming	-	±0.5	-	
V_{CM}	Input bias current	-40℃~105℃	-0.1	-	VDD-1.5	V
I_B	Input offset current	V_{SENSE}=0mV	-	10	-	pA
I_{OS}	Input offset voltage	V_{SENSE}=0mV	-	10	-	pA
V_{HYS}	Input hysteresis voltage	VDD=2.1~5.5V, V_{IN+}=0.5V	-	0 ±10 ±20 ±60	-	mV
Output characteristic						
V_{OH}	Maximum output voltage	-40℃~105℃	-	-	VDD	V
V_{OL}	Minimum output voltage	-40℃~105℃	0	-	-	V
Frequency characteristic						
A_{OL}	Open loop gain	-	-	85	-	dB
BW	Bandwidth	-	-	120	-	MHz
PSRR	Power rejection ratio	VDD=2.1~5.5V,V_{IN+}=1V, V_{SENSE}=0mV	-	80	-	dB
CMRR	Common mode rejection ratio	VDD=2.1~5.5V, -40℃~105℃	-	90	-	dB
Transient characteristic						
T_{STB}	Stable time	-	-	-	1.5	μs
T_{PGD}	Response delay	V_{COM}=1V, V_{IN+}= V_{IN-} ±0.1V	-	50	100	ns

4.10 EFT electrical characteristic

Symbol	Parameter	Condition	Level
V_{EFTB}	Fast transient voltage burst limits to beapplied through 0.1Uf(capacitance) on VDD and VSSpins to induce a functional disturbance	T_A = + 25°C HSI=8MHz, conforms to IEC 61000-4-4	4B

Note: EFT performance is closely related to system design, including power structure, circuit design, the layout, chip configuration and program structure. EFT parameters in above table are internal testing result in CMS, not suitable for all application environments. These parameters are for reference only. System design has influence upon EFT performance. For some special application which needs high EFT performance, please try to avoid interference sources affecting the system when designing. It is suggested to analyze interfering path and optimize design in order to achieve the best anti-interference performance.

4.11 ESD electrical characteristic

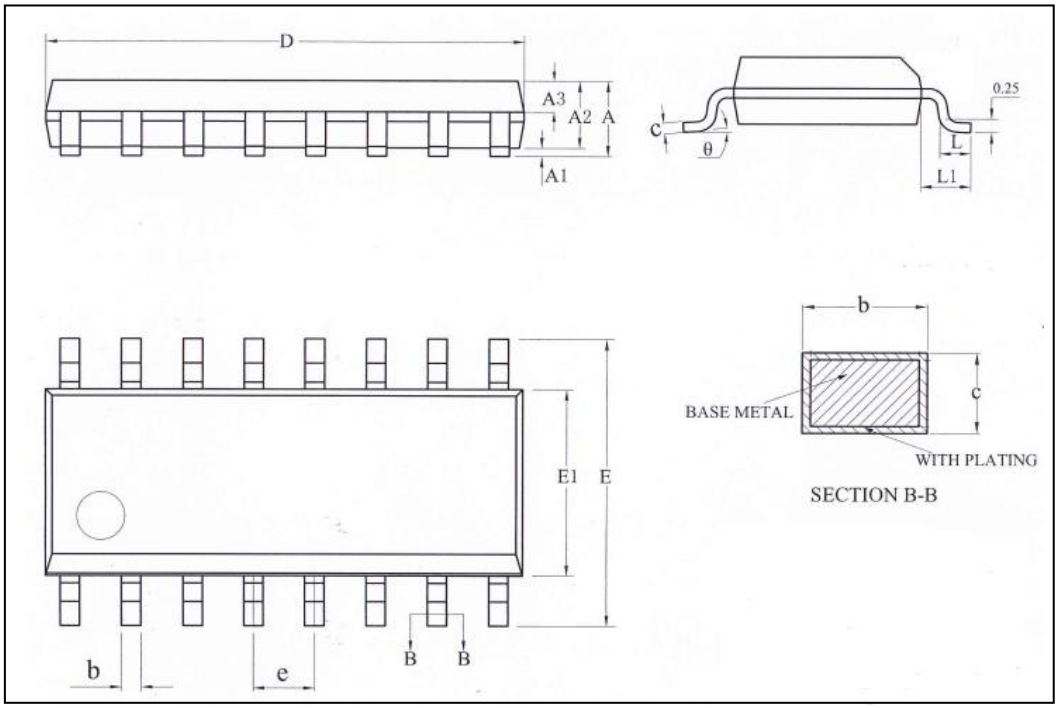
Symbol	Parameter	Condition	Level
V_{ESD}	Electrostatic discharge (human body model HBM)	T_A = + 25°C, JEDEC EIA/JESD22- A114	3B
	Electrostatic discharge (Machine discharge model MM)	T_A = + 25°C, JEDEC EIA/JESD22- A115	C

4.12 Latch-up electrical characteristic

Symbol	Parameter	Condition	Type
LU	Static latch-up class	JEDEC STANDARD NO.78D NOVEMBER 2011	Class I (T_A = +25°C)

5. Package Information

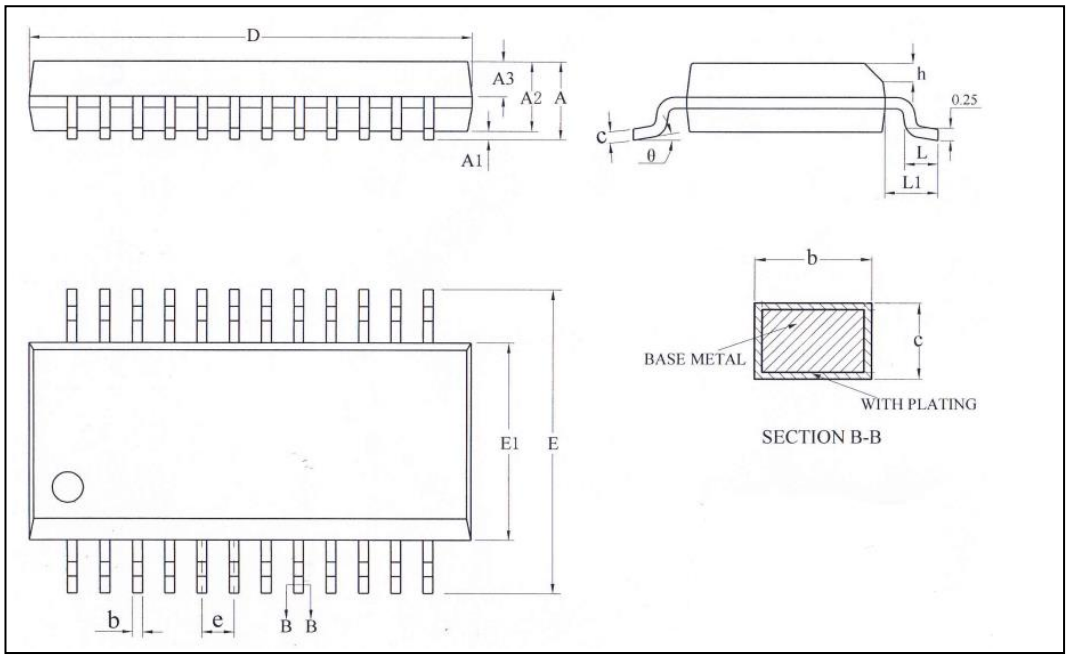
5.1 SOP16



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.75
A1	0.05	-	0.25
A2	1.30	-	1.60
A3	0.60	-	0.71
b	0.356	-	0.47
c	0.20	-	0.26
D	9.70	9.90	10.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
L	0.40	-	0.80
L1	1.05REF		
θ	0	-	8°

Caution: Package dimensions do not include mold flash or gate burrs.

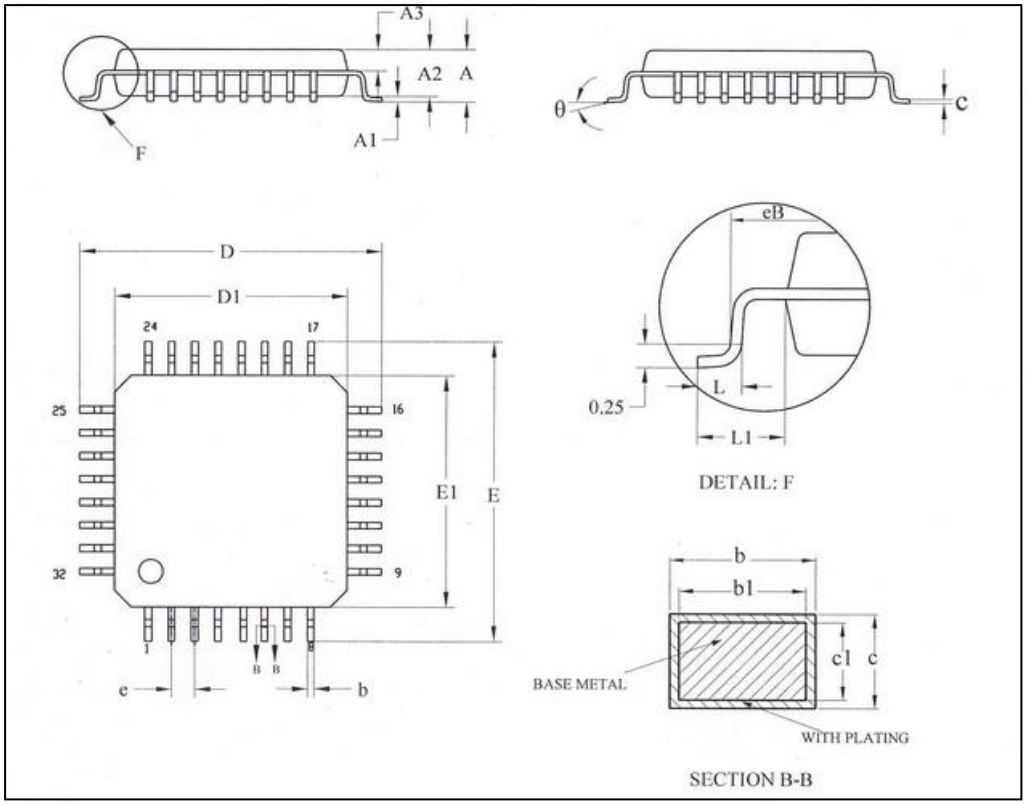
5.2 SSOP24



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.80
A1	0.10	0.15	0.25
A2	1.30	-	1.55
A3	0.60	0.65	0.70
b	0.20	-	0.31
c	0.20	-	0.24
D	8.53	-	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	-	0.50
L	0.406	-	0.889
L1	1.05REF		
θ	0	-	8°

Caution: Package dimensions do not include mold flash or gate burrs.

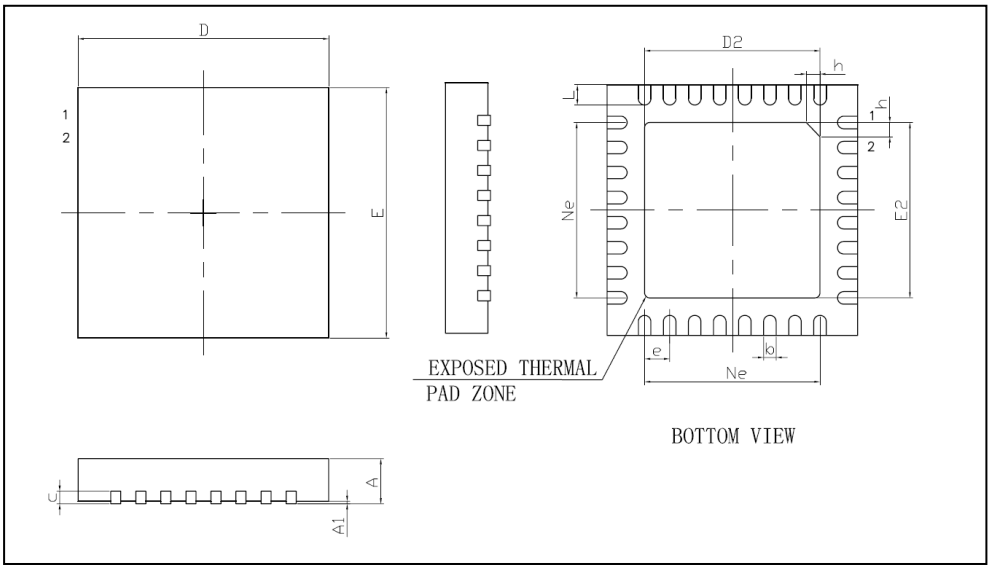
5.3 LQFP32



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.32	-	0.43
b1	0.31	0.35	0.39
c	0.13	-	0.18
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.80BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7°

Caution: Package dimensions do not include mold flash or gate burrs.

5.4 QFN32（5*5*0.75-0.50）



Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	-	3.75
e	0.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	-	3.75
L	0.30	-	0.45
h	0.30	0.35	0.40

Caution: Package dimensions do not include mold flash or gate burrs.

6. Revision History

Version	Date	Revision content
V1.00	July 2019	Initial version
V1.01	August 2019	Modified SSOP24 information and some function descriptions
V1.02	September 2019	1) Modified some register descriptions in UART/SSP. 2) Added SOP16 pin map and related package information. 3) Unified register format
V1.03	December 2019	Modified CCP module capture input selection channel
V1.05	February 2020	Modified pin function description
V1.06	February 2020	Modified some register descriptions Corrected some errors in the package diagram
V1.07	April 2020	Added register description for the user configuration area.
V1.08	July 2022	Deleted the CCP0A function associated with P30.
V1.0.9	May 2023	1) Corrected 5.3 LQFP32 package dimension. 2) Corrected unit format 3) Optimized Sections 4.10, 4.11, 4.12 4) Modified Sections 3.13.4, 3.13.5.2 5) Removed previous 0 op-amp n-regulation enable control registers.
V1.1.0	November 2023	1) Corrected 3.8.5.3 EPWM control register (CON). 2) Modified the description of FLASH electrical parameters in Section 4.6.
V1.1.1	January 2024	1) Revised section 3.4.3 2) Revised the SWD pin in sections 1.3.6, 1.3.7, 2.5.3.
V1.1.2	April 2024	1）Updated QFN, LQFP pin map formats 2）Deleted the stop mode in 1.1 3）Revised 2.4.2 operating mode table. 4）Revised 2.5.3.6 PCON register description. 5）Modified 2.8.2.4 SCR register description. 6）Revised Section 3.1.3.6 and deleted stop mode. 7）Revised 4.2 D.C. electrical characteristic and deleted the stop mode current. 8）Modified 3.1.5.12 GPIOxDIDB register description.
V1.1.3	September 2024	1) Updated 4.8 Common mode input voltage Range values 2) Revised the cover page 3) Modified SOP16/SSOP24/LQFP32/QFN32 package dimensions